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A NEW METHODOLOGY FOR DUTY CYCLE CORRECTION IN 90NM ASIC DESIGNS: ANALYSIS AND IMPLEMENTATION

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***ABSTRACT*:**

This paper presents the analysis and design of a clock signal duty cycle measurement and correction circuit, which is implemented using 90nm ASIC technology. In digital systems, the clock signal plays a crucial role in synchronizing operations across various components. Even minor deviations in the duty cycle can lead to timing violations, setup and hold time failures, increased jitter, and degraded overall performance. Particularly in high-speed and low-power digital circuits, maintaining a 50% duty cycle is critical to ensuring symmetrical timing windows and reducing dynamic power consumption.

INTRODUCTION

In this approach duty cycle measurement and correction circuit, implemented using 90nm ASIC technology. In digital systems, the clock signal plays a crucial role in synchronizing operations across various components. This will affect the operation of sub blocks like DRAM's, dynamic/domino pipelined circuits, pipelined analog-to-digital converters (ADC) and serializer/deserializer (SERDES) clock signal. To avoid these kind of conditions designers are using duty cycle correction circuits. Before feeding the clock to sensitive parts the clock signal will travel through the measurement system and if it is required then it will be taken to the correction area. This is the main idea behind the design[1].

The scope of this study on duty cycle correction circuits encompasses design methodologies, implementation strategies, and performance evaluation. It includes a detailed investigation into how factors such as process variations, signal amplitude, and operating frequency influence the functionality and reliability of these circuits. The study also explores various correction techniques, highlighting the trade-offs between digital and analog approaches. In particular, it compares the accuracy, power efficiency, and integration complexity of digital duty cycle correction circuits against conventional analog solutions, aiming to identify the most suitable architecture for modern high-speed and low-power digital systems.

a)Objectives

- To explore and analyze various duty cycle correction circuits employed in digital systems.
- To gain a comprehensive understanding of the working principles and key components involved in duty cycle correction.
- To analyze and compare various duty cycle correction (DCC) architectures, quantifying their efficacy in neutralizing signal distortions across diverse operating conditions.
- To evaluate the impact of duty cycle deviations on the performance, timing, and reliability of digital circuits.
- To provide design recommendations and propose improvements for the efficient duty cycle correction circuit implementation in modern digital architectures.

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SYNTHESIS

Placement can be done mainly in two phases – Global placement and detailed placement by global placement standard cells will placed inside roughly, at this stage there can be overlapping of the standard cells. By the detail placement the standard cells will be placed InSite rows, i.e. legalize placement. Cost functions includewire length, wire routability, hotspots, performance etc.

a) FORMAL VERIFICATION

The primary objective of formal verification is to ensure that a given design meets specified requirements, properties, or constraints. It leverages a combination of algorithmic and logical techniques to rigorously analyze the correctness of digital blocks, such as ASIC components or entire SoCs, thereby enhancing design reliability and reducing the risk of functional errors.

b) ANALYSIS OF TIMING PATHS

Timing analysis is performed by categorizing the design into distinct paths based on defined start and end points. The start point of a timing path can include elements such as a clock source, a sequential cell (like a flip-flop), a primary input port, the data pin of a level-sensitive latch, the clock input of a sequential element, or a pin with specified input delay. The end point may include a clock, a sequential cell, a primary output port, a pin with output delay, or the data input of a sequential cellcell[1].

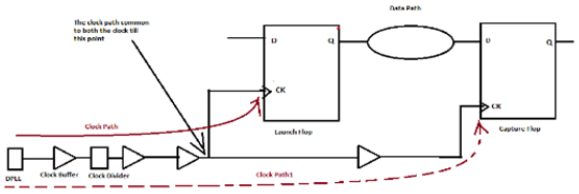

Fig 1-Clock Path diagram

To get some additional advantages, clock path might be passed through a gated element. The definitions and characteristics of the clock varies accordingly in this case. We refer this kind of clock path as gated clock path. In the following Fig.1.

It is level triggered pins and will be able to start out performing at any time of data. So, we can say that in other way that, this path is not in synchronous with rest of circuit and that is the limit we are mentioning Such kind of path an asynchronous path. During timing analysis reports we generally use a few more types of paths and those are the subset of the paths that are mentioned above with some specific characteristics

- Critical Timing path
- Longest Timing Path
- Shortest TimingPath
- Single Cycle path

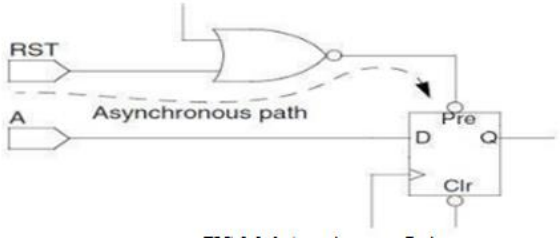

Fig 2 –Asynchronous Path

ANALYSIS OF DELAY IN TIMING PATHS

Net delay and Cell delay and net delay are the two major types of Delay. NET DELAY Net delay occurs between a load pin and driver pin. We need three valuable information to calculate the net delay. Load characteristics of receiver cell, Characteristics of driver cell and RC value of the net are those factors CELL DELAY Cell delay is introduced between an input pin and output pin of a cell. we will get the information of cell delay from the library

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of the cell. We can calculate both the delays in different ways. It mostly depends on the stage which we need information within the design. That is either signoff timing or post layout or pre layout. Depends on the stage we can select the way to calculate the delays. This is because, we need precise value sometimes and approximate value is enough[2].

a) ***16:1 MUX***

A 16:1 MUX (multiplexer) is a digital circuit that selects one of sixteen input signals and passes it to the output based on the value 34 of a control signal. The control signal determines which input signal is selected and passed 35 to the output. The 16:1 MUX can be built using multiple levels of smaller MUXes, such as 2:1 MUXes[3].

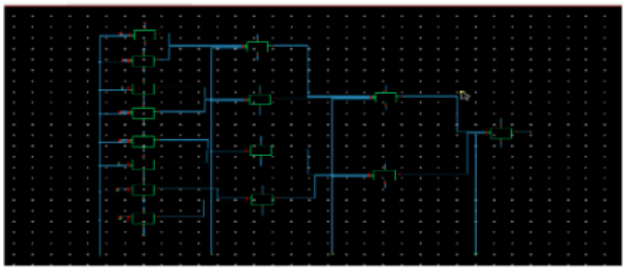

Fig.3. 16:1 MUX Schematic

b) FIXING OF VIOLATIONS

There are many ways to fix the setup and hold violation. These both are dependent to each other, so that to fix setup, we need to do the opposite of fixing hold.For example., we can fix the setup the path by removing the buffer and for fixing the hold, we need to add buffer.

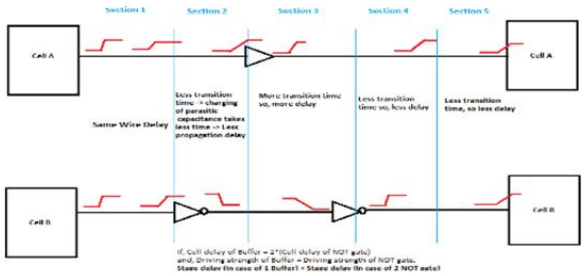

Fig.4. Adding Two Inverter for Timing Fix.

It is increasing the driver size.so that it also called upsizing. But one of the disadvantages of this method is power consumption will be high and total area in the layout is more[4].

- HVT swap

Transition time can be reduced by decreasing threshold voltage and thereby we can reduce the propagation delay. But leakage power will increase. That is the disadvantage of this method.

- Add repeaters.

Since the gate delay is small compared to RC delay, this method is better in the case of delay. Will split path into many small pieces and inset repeaters.

DUTY CYCLE ADJUSTER

The The duty cycle adjuster serves as the architectural core of ASIC-based correction loops, providing the necessary mechanism for pulse-width manipulation

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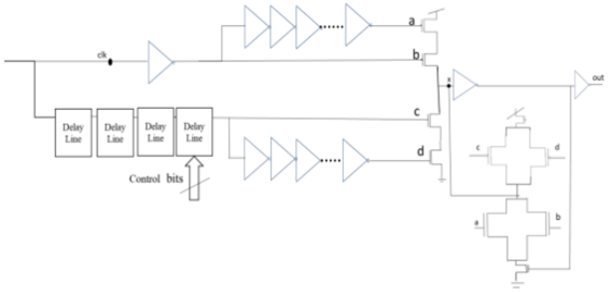

Fig.5. Circuit Diagram of duty Cycle Adjuster

For example, four levels of 2:1 MUXes can be used to build a 16:1 MUX with sixteen inputs. In this configuration, the first level consists of four 2:1 MUXes that select between four pairs of inputs. The second level consists of two 2:1 MUXes that select between two pairs of outputs from the first level. The third level consists of one 2:1 MUX that selects between two outputs from the second level. Finally, the fourth level consists of one final 2:1 MUX that selects between the two outputs from the third level and passes it to the output. The operation of a 16:1 MUX can also be represented using a truth table, which shows the output for all possible combinations of inputs and control signals. The truth table for a 16:1 MUX with inputs A0-A15, control signals C0-C3, and output Y is as follows:

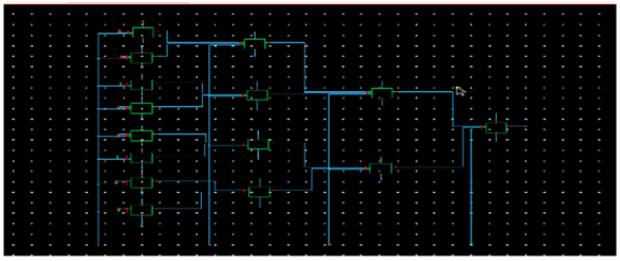

Fig.6. 16:1 Mux Schematic.

DELAY LINE

A delay line is a circuit that introduces a time delay into a signal. It is commonly used in digital circuits to synchronize signals or to introduce precise timing delays. A delay line can be implemented using various techniques, such as RC circuits, inductors, or digital logic gates.

In digital circuits, a delay line can be used to compensate for propagation delays caused by wires and other components in the circuit. The delay introduced by the delay line can be adjusted by changing the number of stages or the characteristics of each stage. For example, in a duty-cycle correction circuit, a delay line may be used to introduce a precise time delay between two complementary signals. This time delay can then be adjusted by changing the characteristics of the individual stages in the delay line. A delay line component in many digital circuits and is used to introduce precise timing delays that are critical for proper circuit operation.

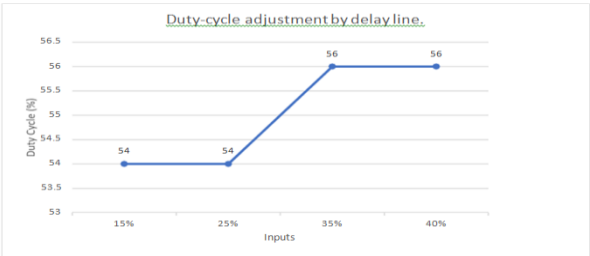

Fig. 7. Graph of Delay line adjustment

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APPLICATIONS

1.High-speed communication systems: In communication systems, accurate timing is essential for transmitting and receiving data.
2.Digital signal processing: In digital signal processing (DSP) applications, accurate timing is important for performing operations such as filtering, modulation, and demodulation. The duty-cycle correction circuit can be used to ensure that the clock signals used in DSP circuits have the correct duty-cycle, which can improve the accuracy and efficiency of these operations.
3. Test and measurement equipment: In test and measurement equipment, accurate timing is important for generating and measuring signals with high precision. The duty-cycle correction circuit can be used to ensure that the clock signals used in these systems have the correct duty-cycle, which can improve their accuracy and repeatability.
4. Overall, the duty-cycle correction circuit systems where accurate timing is critical.

CONCLUSION

The duty cycle correction and measurement circuit was successfully designed, implemented, and tested, yielding promising results. This study has thoroughly explored the concept, functionality, and significance of duty cycle correction in the context of ASIC design. The findings highlight the critical role such circuits play in maintaining clock signal integrity, thereby enhancing the overall reliability and performance of digital systems. The results validate the effectiveness of the proposed design and reinforce the need for robust duty cycle correction techniques in modern high-speed integrated circuits.

Table 1 : Duty Cycle Configuration

MAXIMUM DUTY CYCLE OBSERVED	CONFIGURATION	DUTY CYCLE ENHANCED
15-62%	0000	47%
35-63%	0000	28%
45-61%	0000	16%
50-62%	0000	12%
15-54%	0100	39%
25-54%	0100	29%
35-56%	0100	21%

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