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DESIGN AND VALIDATION OF A 1300 W HIGH-FREQUENCY PFC–LLC BATTERY CHARGER FOR 48 V LIFEPO₄ ELECTRIC VEHICLE PACKS

Ms. Meena Andure[1], Prof. Neha A Zope[2], Mr. Om Naik[3]

[1]Department of Mechanical Engineering, School Of Engineering and Sciences, MIT ADT University, Rajbaug, Loni Kalhor, Pune – 412201, India
meenahattarge@proton.me
[2]Department of Mechanical Engineering, School Of Engineering and Sciences, MIT ADT University, Rajbaug, Loni Kalhor, Pune – 412201, India
neha.zope@mituniversity.edu.in
[3]Department of Mechanical Engineering, School Of Engineering and Sciences, MIT ADT University, Rajbaug, Loni Kalhor, Pune – 412201, India
omravikantnaik@gmail.com

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***ABSTRACT*:**

Electric vehicles require the development of efficient and reliable on-board and off-board chargers. These chargers should be able to ensure the safe operation of the vehicle's battery. In this paper, the design and validation of a 1.3 kW high-frequency switched-mode power supply (SMPS)-based electric vehicle battery charger with a wide input voltage range of 190 V to 265 V AC and a closed-loop control for the regulation of the DC-link voltage and the control of the battery charging process are presented. The proposed charger configuration includes a continuous conduction mode (CCM) active power factor correction (PFC) boost converter for current regulation, a high-frequency LLC resonant DC–DC converter for galvanic isolation, and zero-voltage switching (ZVS) of the converter. The proposed charger is designed to operate at a 51.2 V nominal battery voltage, a maximum battery charging voltage of 58.4 V, and a maximum charging current of 20 A. The control strategy of the proposed charger comprises a multi-loop control strategy with a DC link voltage control loop and a current control loop for the PFC converter, a constant current/constant voltage control strategy for the battery charger circuit, and a frequency modulation control strategy for the LLC converter circuit. The analytical results show that the input power factor is always greater than 0.98, and the efficiency is always greater than 93%. It is also shown that the output voltage ripple is within 1%, and the output current ripple is within 2.5%. Various protection schemes are provided for input over current protection, output over voltage protection, under voltage protection, overload protection, and earth leakage protection. The proposed high-frequency PFC–LLC structure provides a compact solution with low switching losses and high efficiency, which is not possible with conventional low-frequency chargers.

***Keywords**: EV charger, switched-mode power supply (SMPS), power factor correction (PFC), LLC resonant converter, CC–CV charging, zero-voltage switching (ZVS), high-frequency power conversion, battery charger design.*

INTRODUCTION

The success of the adoption of EVs is not only dependent on the development of battery technology but also on the existence of credible, fast, and intelligent systems for charging electric vehicles [5, 6]. With the increase in the number of EVs, the charging system must be improved to meet the rise in power consumption, user convenience, stability of the power grid, and international standardization that must be maintained [7, 8]. This has made EV charging technologies one of the areas of interest in research in power electronics and smart grids.

The selection of the 16 cell series Lithium Iron Phosphate (16S) pack as the reference load, with a nominal voltage of 51.2 V, end of charge voltage of 58.4 V (3.65 V per cell), minimum discharge voltage of 35 V, and a maximum charging current of 20 A with a peak power of 1300 W, is market oriented. The selection of the 16S type with a nominal voltage of 51.2 V has become the standard battery configuration for light electric vehicle energy storage systems because of the flat 3.2 V/cell Lithium Iron Phosphate chemistry, discharge plateau, thermal stability, and cycle life of more than 3000 cycles at 80% depth of discharge [25, 26]. The 48 V battery technology platform has emerged as the preferred choice over NMC and NCA battery technologies in the transportation sector [1]. In the

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industry, the 48 V technology platform is gaining widespread acceptance. As of 2024, the market size for 48 V battery systems was approximately USD 4.2 billion and is expected to skyrocket to around USD 51.5 billion by 2035. From a grid-connectivity perspective, maintaining a power factor of above 0.98 and total harmonic distortion of below 4% will ensure that the charger complies with the EN 61000-3-2 Class A harmonic current emission limits [28], which is a non-negotiable criterion for any AC-powered device sold in Europe and India, and is a critical requirement for approval and grid protection [3]. The proposed charger, with a power rating of 1300 W, directly addresses the requirements of the rapidly expanding electric two- and three-wheeler market. In India alone, more than 850,000 units of electric two-wheelers were sold in 2023, with annual growth rates exceeding 30% under the FAME-II scheme. The electric two-wheeler industry predominantly uses 48 V (16S) LiFePO4 battery configurations of 20 Ah capacity, which directly corresponds to the power rating and voltage window of the charger under consideration. The LiFePO4 EV battery market was valued at USD 5.2 billion in 2024 and is expected to increase to USD 20.4 billion by 2033, with a CAGR of 16.6% during the forecast period [27]. This trend clearly indicates that any charger for 16S LiFePO4 packs is aimed at the single largest market segment of the rechargeable battery industry. As such, the proposed charger is aimed at the largest market segment of the electric vehicle industry that uses 48 V/51.2 V/16S LiFePO4 batteries and requires a 1–1.5 kW charging solution, across the 35–65 V window, demanding precision voltage control and a comprehensive protection scheme [2].

Two-stage designs combining PFC with an isolated DC–DC converter distinguish between the functions of power factor correction, galvanic isolation, and output regulation [19, 20]. In the DC–DC part of the design, operating at kilowatt power levels, the LLC resonant converter is preferred because it can support zero-voltage switching on the primary and zero-current switching on the secondary rectifiers without using lossy snubber circuits [3]–[5].

This paper offers a detailed design resource. It includes annotated circuit diagrams for each stage and component selection for each stage, along with simulation results for key parameters related to electric charger performance. The AC–DC front-end design is the first-level design choice in any onboard battery charger (OBC), as it directly affects power factor correction, harmonic distortion, galvanic isolation, efficiency, and regulatory compliance [34, 35]. The literature reports various single-phase OBC designs, from simple uncontrolled rectifiers to more complex multi-stage soft-switched AC–DC front-ends. Each design choice weighs component count, control complexity, efficiency, and regulatory requirements differently. To assist in selecting an AC–DC front-end design for the proposed 1300 W/48 V OBC charger, various common AC–DC front-end designs and their suitability for the proposed charger requirements (listed in Table I) are reviewed and compared.

A. Uncontrolled Diode Bridge Rectifier

The simplest arrangement is the full bridge rectifier diode that includes a bulk capacitor. This design conducts current on the AC mains only around the peaks of the voltage waveform, so the line current waveform shows poor waveform with a large harmonics content, and the total harmonic distortion (THD) is normally above 80% and the displacement power factor is around 0.55–0.65 [6]. Though this design is extremely inexpensive and has very high reliability, as no power electronics are required, and it uses only diodes and bulk capacitors, it fails to meet the harmonics current limits of the EN 61000-3-2 Class A standard on equipment ratings above 75 W.

Further, the uncontrolled rectifier provides no control of voltage or galvanic isolation, and the rectifier output voltage ripple is predetermined to be twice the mains frequency. Thus, it cannot be operated as a regulated 1300 W battery charger that varies in accordance with IEC 62368-1 and EN 61000-3-2 standards [28].

B. Single-Stage Integrated PFC AC–DC Converter

To bring together power factor correction, galvanic isolation, and output voltage regulation into one conversion stage, single-stage AC–DC converters are depicted in literature. This reduces the number of parts, PCB size, and cost, in comparison with two-stage power supplies [7]. Single-stage AC–DC converters are of various types (such as single-stage flyback with PFC, SEPIC-derived isolated converters, Cuk based isolated PFC converters, and resonant single-stage AC–DC converters). The most important advantage of single-stage AC–DC converters is that no capacitor bank or a second-stage DC–DC converter are required. The power factor correction and output voltage regulation, however, have a conflict of interest. The DC link capacitor is subjected to non-reliable voltage stress depending on the line voltage and load current and may be as high as 500–800 V at light loads. Hence, single-stage AC–DC converters are not so desirable. Such high range in the intermediate bus voltage leads to the conversion ratio between the output-stage switches having a wide and impractical range, limiting the efficiency

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to 87–90% and making THD below 5% hard to achieve across the entire input voltage range of 190–265 V AC. So, the use of single-stage PFC AC–DC converters is more limited to power supplies of usually up to 200 W, in which case efficiency is not a critical issue [5].

C. Two-Stage: Boost PFC + Phase-Shifter Full-Bridge DC–DC Converter

In the two-stage configuration depicted, the AC PFC and DC isolation/voltage conversion are separated to allow independent optimization of each aspect. Stage 1 uses a standard CCM Boost PFC operating at 100 kHz, with a sinusoidal input current from the rectified mains and a constant DC link at 400 V. This results in a power factor of above 0.98 and total harmonic distortion of below 5% over the entire input voltage range [8]. The 400 V DC link from the PFC stage is a clean, low-ripple source for Stage 2.

For Stage 2, the phase-shifter full-bridge (PSFB) converter is again the preferred solution at this power level. This is because PSFB can provide zero-voltage switching for all four active switches by leveraging the leakage induction of the transformer during dead times. At full load with a 400 V DC link, the PSFB converter's efficiencies are measured to be around 91–93% [1]. However, ZVS is also observed to be lost for the leading-leg switches when the load reduces to around 30–40% of the full load value, since there is not enough leakage energy left to discharge the switch's output capacitance during dead times. Another limitation of PSFB is that the duty-cycle loss during the freewheeling period causes a circulating current on the primary side, which does not contribute to power transfer, thus increasing conduction losses—especially in topologies that need a high turns ratio to step down from 400 V to 58.4 V.

As such, the PSFB converter has relatively lower partial-load efficiencies compared to the LLC resonant converter, which is a major drawback for a battery charger that spends a large portion of its duty cycle at partial loads during the CV mode.

D. Bridgeless Totem-Pole PFC + LLC Resonant Converter

The bridgeless totem-pole PFC configuration removes the input diode bridge completely. This is achieved by utilizing the two slow-switching diodes in the totem-pole PFC circuit as the rectifiers for each half-cycle of the AC input, and using the two fast-switching GaN devices for the continuous conduction mode boost PFC. The removal of the four forward drops of the diode bridge (approximately 4×0.7 V = 2.8 V at 7 A input RMS current) reduces losses by approximately 1.5–2.0 percentage points over the conventional diode-bridge boost PFC, achieving Stage 1 efficiencies in the 98–99% range. With a half-bridge or full-bridge LLC resonant converter in Stage 2, the two-stage system can achieve efficiencies of 95–97%.

The fast-switching circuit must contend with bidirectional current flow and the MOSFET body diode reverse recovery effects during switching [13, 14]. Therefore, this configuration is not recommended for use with Si MOSFETs, but with GaN or SiC devices instead [14]. Second, the control circuitry must be able to sense the AC zero crossings and transition smoothly between the positive and negative half-cycles without distorting the waveforms with dead time effects, or else the THD will increase significantly [13, 15].

TABLE I — Topology Comparison for 1300 W / 48 V

E. Proposed Topology: Two-Stage Diode-Bridge Boost PFC + Full-Bridge LLC Resonant DC–DC Converter

As a result, we can now put it all together. The topology proposed is a two-stage solution. Stage 1 is a traditional diode-bridge boost PFC topology that maintains a high power factor (PF > 0.98), minimizes total harmonic distortion below 4%, and produces a stable 400 V DC output voltage with a ripple of less than 2%. These results are compliant with EN 61000-3-2 Class A standard requirements [28]. The diode-bridge boost topology is a great solution for Stage 1 as it is easy to implement an average current mode control strategy. Stage 2 is a full-bridge LLC resonant DC–DC converter. The series resonant capacitor Cr is introduced to complete the Lr–Cr–Lm resonant tank. The LLC resonant topology enables full ZVS for all four primary switches as well as full ZCS for both secondary rectifiers at resonant frequency fr without requiring additional passive components or lossy snubber circuits [3, 4]. Moreover, a sinusoidal primary current is achieved at switching frequency fs equal to resonant frequency fr. The LLC resonant topology eliminates circulating currents that are present in a PSFB topology. The output voltage regulation is achieved by modulating fs around fr using an LLC resonant controller from ON Semi, namely NCP1399, to regulate the output voltage over the 35–65 V range corresponding to a full LiFePO4 CC/CV battery charging curve. Figure 1(f) shows a comparison of different topologies that proves that

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the proposed two-stage solution meets the requirements of PF > 0.98 and η > 93%, while at the same time it has a practical and proven topology.

SYSTEM SPECIFICATIONS

A. Electrical Specifications

The charger is designed to operate from the single-phase AC mains across the full range of 190 V to 265 V at 50 Hz, which covers both the nominal Indian/European 230 V supply and the ±15% tolerance band mandated by IEC 60038. The intermediate 400 V DC bus is regulated by the PFC stage and held constant regardless of input voltage variation; the LLC stage then steps this down to the 35–65 V output window required by the LiFePO4 CC/CV charging profile. Maintaining a stable DC bus is not just a design convenience—it is what allows the LLC converter to operate consistently near its resonant frequency, ensuring ZVS and ZCS conditions are preserved across the load range [1, 3].

Table II lists every electrical parameter with its target value. The power factor specification of greater than 0.98 and the THD limit of below 5% at full load are not arbitrary—they are set to comply with EN 61000-3-2 Class A harmonic emission limits, which are mandatory for any AC-powered equipment above 75 W sold in the European Union and increasingly enforced in India under the Bureau of Indian Standards [28]. Below these levels, the charger is a well-behaved load on the grid; above them, it would require additional filtering at the system level and could cause distribution transformer heating in high-density EV charging installations.

For clarity, three different standards govern three distinct aspects of this design. EN 61000-3-2 governs harmonic current emissions from the AC input — it is the standard this charger must meet to be sold in Europe. EN 55032 governs conducted and radiated electromagnetic interference (EMI) limits at the mains terminal — compliance is achieved by the Stage 2 EMI filter design. IEC 62955 defines earth leakage protection requirements for EV charging equipment — it sets the 8 mA AC trip threshold implemented by the differential current transformer in the protection architecture [28, 30].

TABLE II — Complete Electrical Specifications

Parameter	Symbol	Value	Unit
Input Voltage Range	V_AC,in	190 – 265	V_AC
AC Power Factor	PF	> 0.98	—
Intermediate Bus	V_bus	400	V_DC
Nominal Charge Voltage	V_nom	51.2	V_DC
Max. Charge Voltage (EoC)	V_EoC	58.4	V_DC
Max. Charge Current	I_max	20 ± 5%	A
Output Voltage Ripple	ΔV_o	< 1% OCV	%
Output Current Ripple	ΔI_o	< 2.5% rated	%
Max. Output Power	P_out	1300 (59V/20A)	W
Efficiency @ 230V, 100%	η	> 93%	%
Output OVP	V_OVP	65	V
Output UVP	V_UVP	35	V
Earth Leakage Trip	I_ELS	8	mA

The output voltage ripple target of below 1% and current ripple below 2.5% are driven by LiFePO4 battery health requirements. Repeated high-frequency charge/discharge micro-cycles from excessive ripple accelerate solid-electrolyte interface (SEI) layer growth and lithium plating at the graphite anode, reducing cycle life. The 47 µH

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output inductor and 940 µF parallel capacitor bank are sized specifically to meet these ripple limits at 100 kHz switching frequency, as shown in the Stage 8 calculations below.

STAGE-BY-STAGE CIRCUIT DESIGN AND ENGINEERING CALCULATIONS

A. Stage 1 — AC Input Protection (Fuse + NTC Inrush Limiter)

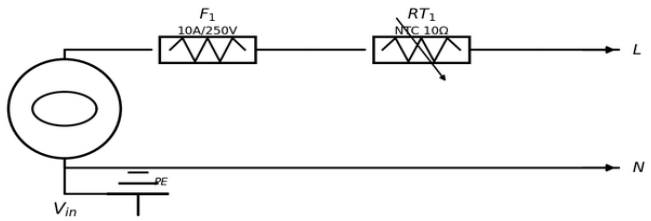

Fig. 1. Stage 1: AC input protection — fuse F1 (10A/250V slow-blow) and NTC thermistor RT1 for inrush current limiting.

The AC supply enters the charger through fuse F1 and an NTC thermistor RT1 connected in series. The job of this front-end stage is straightforward but important: protect the downstream components from the large inrush current surge that occurs the moment power is applied to an uncharged bulk capacitor bank. At power-on, the bulk electrolytic capacitors at the PFC output look like a short circuit to the AC source. Without current limiting, the initial charge current would be limited only by the impedance of the mains supply and PCB traces—easily exceeding 100 A peak, which would stress or destroy the rectifier diodes and damage the PCB conductors [20].

An NTC thermistor works on a straightforward principle: cold resistance (10 Omega at room temperature) drops sharply as the device self-heats under current flow. At power-on, those 10 Omega hold the inrush peak to 32.5 A, well inside the fuse I2t margin. Within a few hundred milliseconds the resistance falls below 0.3 Omega. The complication is steady-state dissipation: at 5.65 A RMS, the device loses 9.6 W continuously, beyond the rating of a standard 3 A NTC. Removing it from the current path via a relay bypass once inrush has settled is the industry-standard fix, documented in Bourns and Vishay Ametherm inrush application notes.

F1 is coordinated with the NTC by specifying a slow-blow I2t rating (125 A2s) well above the measured inrush energy (10.6 A2s), so the fuse rides through the controlled start-up surge. On a genuine sustained fault such as a shorted X-capacitor or a failed EMI choke winding, the slow-blow time-current characteristic still delivers reliable clearance [29].

Engineering Calculations

$$I_{pk,inrush} = V_{AC,peak} / R_{NTC,cold}$$
$$= 325 / 10$$
$$= 32.5\ A\ (cold\ start\ peak) \quad ...(1)$$

$$I^2t_{inrush} = I_{pk}^2 \times t_{inrush}$$
$$= 32.5^2 \times 0.01$$
$$= 10.6\ A^2{\cdot}s \ << \ I^2t_{fuse}\ (125\ A^2{\cdot}s)\ \checkmark \quad ...(2)$$

$$P_{NTC,steady} = I_{rms}^2 \times R_{hot}$$
$$= (5.65)^2 \times 0.3$$
$$= 9.6\ W \quad ...(3)$$

⚠ 9.6 W exceeds the continuous power rating of the 3 A NTC. Per Bourns inrush application note and Vishay Ametherm guidance, either a higher-rated NTC (≥6 A, e.g. Ametherm MS32 10003) or a relay-based bypass circuit must short out the NTC after startup to prevent sustained thermal stress on the device.

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Components: F1 — Littelfuse 327010, 10 A / 250 V slow-blow ceramic. RT1 — Ametherm SL22 10003, 10 Ω / 3 A rated.

B. Stage 2 — EMI Filter (CM Choke + X/Y Capacitors)

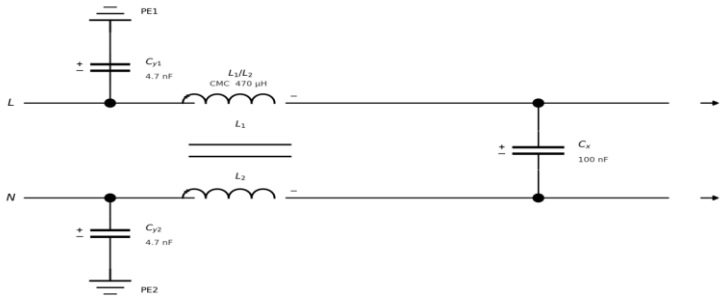

Fig. 2. Stage 2: EMI filter comprising common-mode choke (CMC) L1/L2, differential X-capacitor Cx (100 nF, X2-class), and Y-capacitors Cy1/Cy2 (4.7 nF, Y2-class) to PE.

Placed between the input fuse and the bridge rectifier, the EMI filter serves two roles: keeping switching noise inside the charger from reaching the mains, and stopping mains-borne disturbances from reaching the control circuits. At 100 kHz switching frequency without any filtering, the conducted emissions would exceed EN 55032 Class B limits by a significant margin — enough to block CE marking and BIS certification in India [28, 29].

The filter combines a common-mode choke (CMC) with X- and Y-class capacitors. The CMC — a bifilar winding on a high-permeability toroid — presents high impedance (295 Ω at 100 kHz) to common-mode currents while letting the differential power current pass through with negligible loss. Cx bridges line to neutral, short-circuiting differential-mode noise back across the supply terminals. Cy1/Cy2 steer common-mode noise to protective earth. Y-capacitor values are constrained by the earth leakage budget: the continuous leakage current through Cy to PE must not approach the 8 mA ELS trip threshold, which sets a practical upper limit of about 78 nF — the selected 4.7 nF sits well within this margin [30].

Engineering Calculations

$$Z_{Cx} = 1 / (2\pi \times f_{sw} \times Cx)$$
$$= 1 / (2\pi \times 100k \times 100n)$$
$$= 15.9\ \Omega \text{ (DM shunt impedance at switching frequency)} \quad ...(4)$$

$$Z_{CMC,CM} = 2\pi \times f_{sw} \times L_{CMC}$$
$$= 2\pi \times 100k \times 470\mu$$
$$= 295.3\ \Omega \rightarrow \text{CM attenuation} > 24\ \text{dB} \quad ...(5)$$

$$C_{Y,max} = I_{leak,max} / (V_{AC,peak} \times 2\pi \times f_{line})$$
$$= 3.5m / (325 \times 314)$$
$$= 34.3\ \text{nF} \rightarrow \text{select 4.7 nF Y2 (safe margin)} \quad ...(6)$$

Components: CMC — TDK ACM7060-900-2PL-TL, 470 µH. Cx — Kemet R463I2100AA1K, 100 nF X2-class. Cy1/Cy2 — WIMA MKP2, 4.7 nF Y2-class.

C. Stage 3 — Bridge Rectifier and Bulk Capacitor

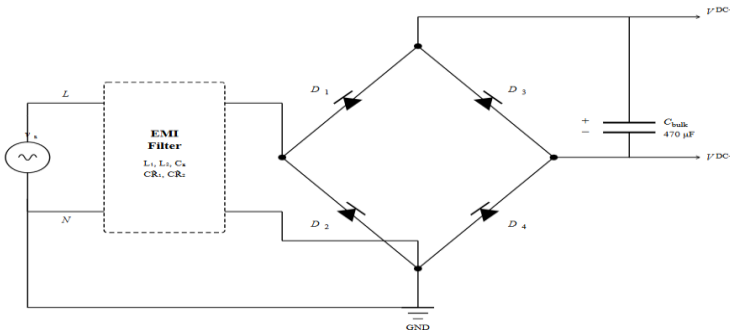

Fig. 3. Stage 3: Full-wave bridge rectifier D1–D4 in diamond configuration, producing pulsating DC from AC mains. C_bulk (470 µF/450 V) provides initial energy storage.

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The full-wave bridge converts mains AC into a pulsating unipolar DC for the PFC stage. D1 and D4 conduct on the positive AC half-cycle; D2 and D3 pick up the negative half-cycle. At the bridge output, C_bulk smooths the pulsating waveform and acts as an energy reservoir: during the intervals when the instantaneous AC voltage falls below the average, the PFC converter draws on stored charge in C_bulk rather than demanding current spikes from the mains.

Each rectifier diode must withstand the peak inverse voltage at maximum AC input, including transient spikes that can reach 50–100% above nominal in mixed industrial/residential supply environments [20]. The calculated worst-case PIV of 374.7 V with 265 V AC input justifies the 600 V rated device, giving a 1.6× margin. Diode RMS current is verified in the calculations below using the correct factor for a CCM PFC input rather than the 1.8× approximation applicable to uncontrolled rectifiers.

Engineering Calculations

$$V_{DC,peak} = \sqrt{2} \times V_{AC,nom} - 2 \times V_f$$
$$= 1.414 \times 230 - 1.4$$
$$= 323.8 \text{ V} \quad ...(7)$$

$$PIV = \sqrt{2} \times V_{AC,max}$$
$$= 1.414 \times 265$$
$$= 374.7 \text{ V} \rightarrow \text{select 600 V rated diodes} \quad ...(8)$$

Diode RMS current (PFC-shaped sinusoidal input):

$$I_{diode,rms} = 0.707 \times I_{in,peak} / \sqrt{2}$$
$$= 0.707 \times 9.97$$
$$= 7.05 \text{ A} << 15 \text{ A rated} \checkmark \quad ...(9)$$

Note: 1.8× factor applies to uncontrolled cap-input rectifiers.
For CCM PFC with sinusoidal current, 0.707× is correct [20].

$$C_{bulk} = I_{out,avg} / (2 \times f_{AC} \times \Delta V_{bulk})$$
$$= 5.12 / (2 \times 50 \times 26.8)$$
$$= 190 \text{ µF} \rightarrow \text{select 470 µF / 450 V (2.5× safety)} \quad ...(9)$$

Components: D1–D4 — Vishay VS-15ETL06-M3 (600 V / 15 A). C_bulk — Nippon Chemi-Con 470 µF / 450 V, 105°C rated.

D. Stage 4 — Active PFC Boost Converter

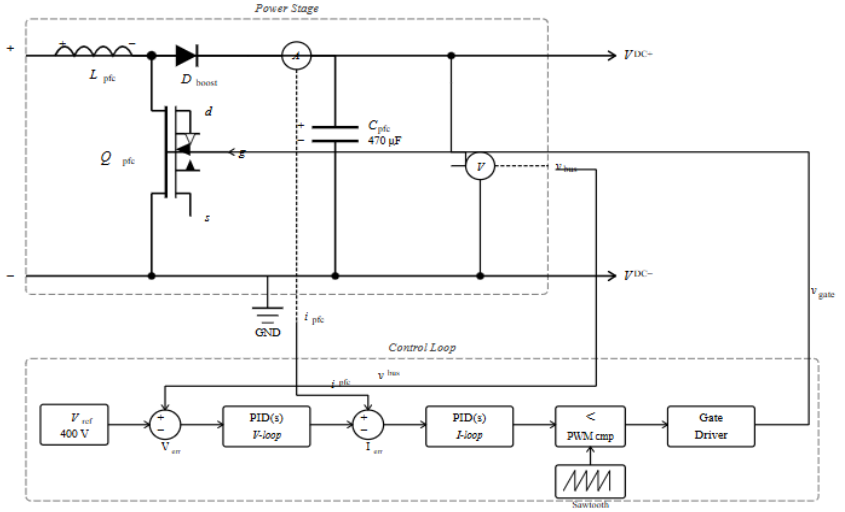

Fig. 4. Stage 4: CCM boost PFC converter. L_pfc (470 µH) and SiC MOSFET Q_pfc operate at 100 kHz. C_pfc (470 µF/450 V) holds the 400 V intermediate bus.

The active PFC boost converter is the most critical stage from a grid power quality standpoint. It is responsible for achieving three things simultaneously: drawing sinusoidal current from the rectified AC supply, maintaining unity power factor (PF > 0.98), and regulating the intermediate DC bus at a stable 400 V regardless of input

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voltage or load variation. The converter operates in continuous conduction mode (CCM) at 100 kHz throughout the full mains cycle, controlled by an average current mode controller with cascaded PI loops—an outer voltage loop regulating V_bus and an inner current loop shaping the inductor current to be sinusoidal and in phase with the AC input voltage [9, 10, 11].

CCM is selected over DCM for a straightforward reason: continuous inductor current produces a smoother AC input waveform with lower peak values for the same average power, translating directly to THD below 4%. A DCM implementation at 1.3 kW would push THD above 10% without considerable additional filtering. At the heart of this stage is the Wolfspeed C3M0065090D SiC MOSFET — 65 mΩ on-resistance and near-zero reverse recovery charge make 100 kHz operation practical in a way that no silicon MOSFET can match at this power level [22].

Inductor sizing drives the current ripple performance. Worst-case occurs at minimum AC input (190 V) and full load — the duty cycle reaches D_max = 0.33 and input current peaks at 9.97 A. Targeting a ripple of 20% of peak current (2.0 A_pp) sets a minimum inductance of 314 µH. The selected 470 µH provides calculated ripple of 1.99 A_pp in this condition and adds useful margin against inductor saturation under transient overload conditions.

Engineering Calculations

$$I_{in,peak} = \sqrt{2} \times P_{out} / (\eta_{PFC} \times V_{AC,min}) = 1.414 \times 1300 / (0.97 \times 190) = 9.97\ A \quad ...(10)$$

$$D_{max} = 1 - (\sqrt{2} \times V_{AC,min} / V_{bus}) = 1 - (268.7 / 400) = 0.33 \text{ (at } V_{AC} = 190\ V, V_{bus} = 400\ V) \quad ...(11)$$

$$L_{pfc} = V_{in,min} \times D_{max} / (\Delta I \times f_{sw}) = 190 \times 0.33 / (2.0 \times 100k) = 314\ \mu H \rightarrow \text{select } 470\ \mu H \quad ...(12)$$

$$C_{pfc} = P_{out} / (2\pi \times f_{AC} \times V_{bus} \times \Delta V_{bus}) = 1300 / (314 \times 400 \times 8) = 515\ \mu F \rightarrow \text{select } 470\ \mu F / 450\ V \quad ...(13)$$

Components: Q_pfc — Wolfspeed C3M0065090D SiC MOSFET (900 V / 36 A, R_DS(on) = 65 mΩ). D_boost — ROHM SCS210KGC SiC Schottky (zero reverse recovery). Controller — ON Semi NCP1654.

E. Stage 5 — Full-Bridge LLC Inverter (H-Bridge)

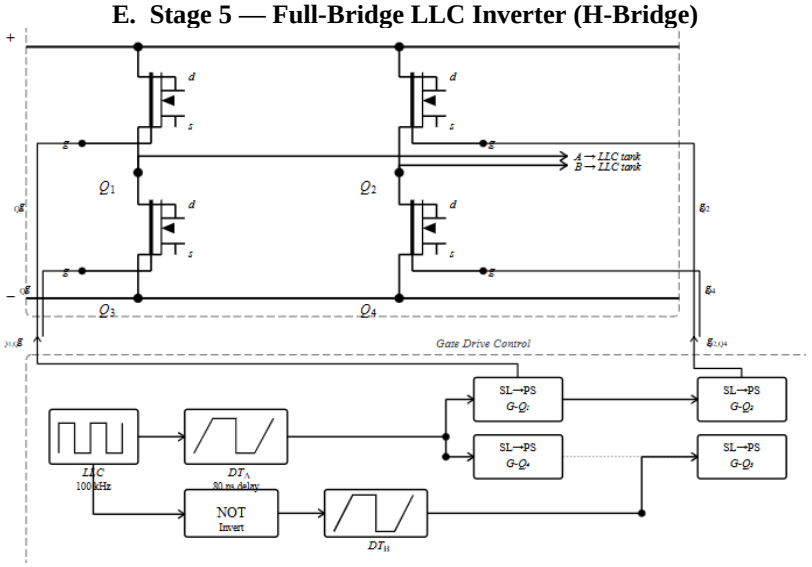

Fig. 5. Stage 5: Full H-bridge inverter using four 650 V GaN MOSFETs Q1–Q4. Diagonal pairs (Q1,Q4) and (Q2,Q3) switch alternately at 100 kHz. Dead-time of 80 ns ensures ZVS.

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The full-bridge H-bridge stage converts the 400 V DC bus into a high-frequency bipolar square wave at the LLC resonant tank input. The four GaN MOSFETs Q1–Q4 operate in two diagonal pairs: Q1 and Q4 conduct simultaneously during one half-period, applying +400 V across the transformer primary; Q2 and Q3 conduct during the other half-period, applying −400 V. The result is a symmetric bipolar square wave at 100 kHz, which is exactly what the LLC resonant tank needs as its input.

The 80 ns dead time between diagonal pair switching is the ZVS enabling interval. During that window, magnetising inductance Lm drives current through the body diodes of the incoming switches, clamping the drain voltage to zero before the gate signal arrives. Turn-on therefore occurs at zero voltage, eliminating the capacitive discharge loss that hard-switching would otherwise cause at every cycle. Equation (17) verifies that the 1.41 A magnetising current fully discharges the 47 pF C_oss of the Nexperia GS-065-030-2-L within the 80 ns window, leaving a 3× margin [13, 14, 21].

GaN is specified here rather than silicon for one overriding reason: Q_rr < 1 nC. Body-diode conduction during dead time is essential for ZVS — with a high-Q_rr silicon MOSFET, the end of the dead time would trigger a hard-commutation spike that destroys the soft-switching action entirely. Beyond reverse recovery, the 30 mΩ on-resistance of the GS-065-030-2-L keeps conduction losses at 1.27 W per switch — a level unachievable with any 650 V silicon device.

Engineering Calculations

$$I_{Q,rms} = (I_{out} / n) / \sqrt{2}$$
$$= (20 / 2.167) / 1.414$$
$$= 6.52\ A \quad ...(14)$$

$$P_{cond/FET} = I_{Q,rms}^2 \times R_{DS(on)}$$
$$= 6.52^2 \times 0.030$$
$$= 1.27\ W \rightarrow \text{total bridge: } 4 \times 1.27 = 5.1\ W \quad ...(15)$$

$$I_{Lm,min} = V_{bus} / (4 \times f_{sw} \times Lm)$$
$$= 400 / (4 \times 100k \times 707\mu)$$
$$= 1.41\ A > 0.60\ A \text{ required for ZVS } \checkmark \quad ...(16)$$

Dead-time check:

$$t_{dead,min} = 2 \times C_{oss} \times V_{bus} / I_{Lm}$$
$$= 2 \times 47p \times 400 / 1.41$$
$$= 26.6\ ns < 80\ ns \text{ set} \rightarrow \text{full ZVS margin } \checkmark \quad ...(17)$$

Components: Q1–Q4 — Nexperia GS-065-030-2-L GaN FET (650 V / 30 A, R_DS(on) = 30 mΩ). Gate driver — TI UCC21220A with 80 ns programmable dead time.

F. Stage 6 — LLC Resonant Tank and High-Frequency Transformer T1

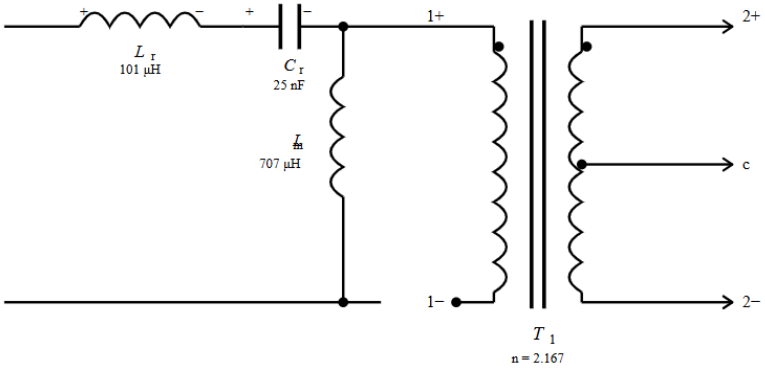

Fig. 6. Stage 6: LLC resonant network — series Lr (101 µH) and Cr (25 nF) form the resonant tank. Transformer T1 (E55/N87 ferrite, 100 kHz, 26:12 turns) provides galvanic isolation.

Three reactive elements define the LLC resonant tank: series inductor Lr, series capacitor Cr, and the transformer magnetising inductance Lm acting as a shunt. Together they produce a frequency-dependent voltage gain curve

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— the key property that allows output regulation by modulating fs around fr without requiring any additional passive components or lossy dissipative elements [1, 3, 5].

Operating at exactly fr gives minimum resonant tank impedance, lowest circulating current, and simultaneous ZVS on primary and ZCS on secondary — conditions for peak efficiency. During the CC charging phase with low battery voltage, fs is pushed above fr into the inductive gain region, deliberately reducing gain to limit current. At end of charge when the battery reaches 58.4 V, fs returns to fr and the full efficiency advantage of resonant operation is recovered during the CV taper phase [4, 7].

The transformer T1 performs three functions: galvanic isolation between the 400 V primary bus and the 35–65 V secondary, the turns-ratio voltage step-down required to reach the output voltage range, and provision of the magnetising inductance Lm that enables ZVS on the primary switches. The transformer is wound on an E55 N87 ferrite core operating at 100 kHz. The N87 material was selected for its low core loss at 100 kHz and 45 mT peak flux density—well below the 390 mT saturation limit, leaving a 8.5× saturation margin. Litz wire is used for both primary and secondary windings to reduce AC copper losses due to skin and proximity effects at 100 kHz [31, 32, 33].

Engineering Calculations

Characteristic impedance:

$$Z_r = 63.5\ \Omega$$

(Selected by design for optimal LLC gain curve shaping and ZVS margin across the full 20–100% load range. Z_r is a design parameter, not derived analytically — consistent with Musavi et al. [1], Ta et al. [3], and Deng et al. [TVT 2014]) ...(18)

$$L_r = Z_r / (2\pi \times f_r) = 63.5 / (2\pi \times 100k) = 101\ \mu H \quad ...(19)$$

$$C_r = 1 / (2\pi \times f_r \times Z_r) = 1 / (2\pi \times 100k \times 63.5) = 25.1\ nF \rightarrow \text{select } 25\ nF \quad ...(20)$$

$$L_m = k \times L_r,\ k = 7 = 7 \times 101 = 707\ \mu H \text{ (built into T1 via controlled air gap)} \quad ...(21)$$

Turns ratio:

$$n = V_{pri,fund} / (2 \times V_{out,max}) = (4/\pi \times 200) / (2 \times 58.4) = 2.18 \rightarrow 26{:}12 \text{ turns } \checkmark \quad ...(22)$$

Core flux density check:

$$B_{peak} = V_{pri} / (4 \times f_{sw} \times N_{pri} \times A_e) = 200 / (4 \times 100k \times 26 \times 420e\text{-}6) = 45.7\ mT << 390\ mT \text{ saturation } \checkmark \quad ...(23)$$

Components: Lr — E42/21/15 N87 core, 45 turns litz wire. Cr — EPCOS B32674 film capacitor, 25 nF. T1 — E55/28/21 N87 ferrite, 26:12 turns litz, Lm = 707 µH.

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G. Stage 7 — Secondary Output Rectifier (Centre-Tap SiC)

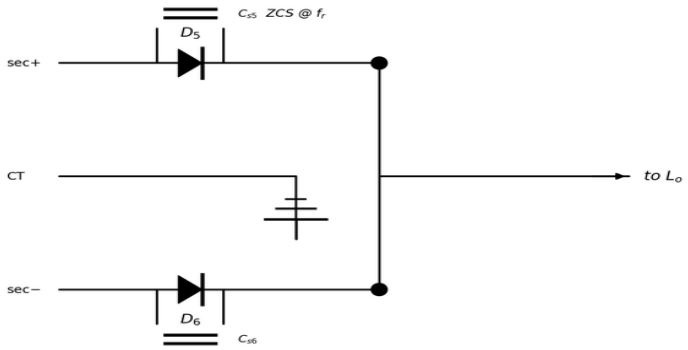

Fig. 7. Stage 7: Centre-tap full-wave rectifier using SiC Schottky diodes D5 and D6 (200 V/20 A). Snubber capacitors (10 nF) across each diode suppress voltage transients.

The secondary rectifier converts the high-frequency AC output of the transformer secondary into DC for battery charging. A centre-tap full-wave configuration is used: the transformer secondary has a centre-tap connected to the positive output rail, and the two outer taps each connect to one SiC Schottky diode (D5 and D6) whose cathodes are joined at the output. Each diode conducts on alternate half-cycles of the LLC switching waveform. At nominal load with fs = fr, the transformer secondary current is sinusoidal and crosses zero at precisely the commutation instant — when reverse voltage would otherwise be applied to the outgoing diode. Natural ZCS results: no forced current interruption, no reverse recovery charge, and no associated loss. SiC Schottky diodes ($Q_{rr} \approx 0$) are used rather than silicon precisely to preserve this characteristic — a silicon diode with significant Q_{rr} would reintroduce hard commutation losses even under ZCS conditions. Snubber capacitors (10 nF) across each diode clamp leakage-inductance voltage spikes to within the 200 V diode rating [3, 22].

At 1.5 V forward voltage and 20 A output current, the two output diodes account for 30 W of dissipation — 40% of the charger's entire loss budget, concentrated in two components. Diode-based rectification has no path to eliminate this loss; only synchronous rectification with GaN MOSFETs (Section VIII) can address it, reducing rectifier loss from 30 W to approximately 6 W.

Engineering Calculations

$$V_{sec,pk} = V_{bus} / (2 \times n)$$
$$= 400 / (2 \times 2.167)$$
$$= 92.3\ V \quad \text{(peak secondary voltage per half-winding)} \quad ...(24)$$

$$V_{out,avg} = (2/\pi) \times V_{sec,pk} - V_f$$
$$= (2/\pi) \times 92.3 - 0.5$$
$$= 58.4\ V\ \checkmark \quad ...(25)$$

$$PIV_{D5,D6} = 2 \times V_{sec,pk}$$
$$= 2 \times 92.3$$
$$= 184.6\ V \rightarrow \text{select 200 V rated diodes} \quad ...(26)$$

$$P_{rect} = V_f \times I_{out} = 1.5 \times 20 = 30\ W \text{ (dominant loss)} \quad ...(27)$$

Components: D5, D6 — ROHM SCS220KGC SiC Schottky (200 V / 20 A, $V_f = 1.5$ V, $Q_{rr} \approx 0$). Snubbers — 10 nF / 200 V ceramic across each diode.

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H. Stage 8 — Output LC Filter and Current Sense

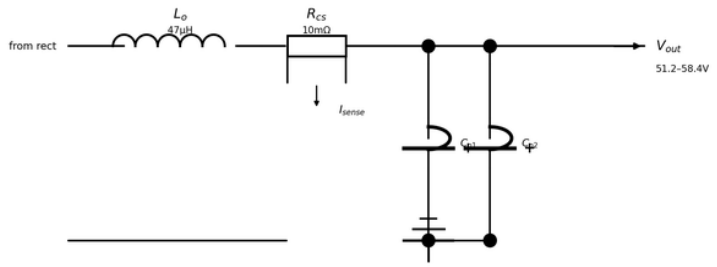

Fig. 8. Stage 8: Output LC filter — inductor Lo (47 μH) limits current ripple; dual capacitors Co1/Co2 (2×470 μF/100 V) limit voltage ripple. Current-sense shunt Rcs (10 mΩ/5 W).

The output LC filter is the final processing stage before the battery terminals. Its job is to reduce the 100 kHz switching ripple on both the output voltage and current to the specified levels—below 1% of open-circuit voltage and below 2.5% of rated current respectively. These limits are not aesthetic requirements: they directly affect battery health. High-frequency current ripple causes localised heating within the battery cells through internal resistance (I^2R), and voltage ripple can push individual cells momentarily above their 3.65 V per cell limit, accelerating capacity degradation [26, 27].

The filter inductor Lo is wound on a powder-iron core chosen for its high saturation current—it must handle 20 A DC bias without significant inductance droop. The dual output capacitors Co1 and Co2 are connected in parallel for two reasons: halving the ESR (which directly reduces high-frequency voltage ripple) and doubling the ripple current handling capability. The current-sense shunt Rcs (10 mΩ) provides the voltage signal used by the CC/CV controller to close the current control loop. Its 5 W power rating ensures it operates well within rating at 20 A: P = I² × R = 400 × 0.01 = 4 W.

Engineering Calculations

$$\begin{aligned} Lo\_min &= V\_out \times (1 - D\_sec) / (\Delta I\_o \times f\_sw) \\ &= 58.4 \times 0.36 / (0.5 \times 100k) \\ &= 42.1\ \mu H \ \rightarrow\ \text{select } 47\ \mu H \end{aligned} \quad ...(28)$$

$$\begin{aligned} \Delta I\_Lo\ @\ 47\mu H &= V\_out \times (1 - D\_sec) / (Lo \times f\_sw) \\ &= 58.4 \times 0.36 / (47\mu \times 100k) \\ &= 0.447\ A\_pp\ \ (<2.5\%\ of\ 20\ A = 0.5\ A)\ \checkmark \end{aligned} \quad ...(29)$$

$$\begin{aligned} Co\_min &= \Delta I\_Lo / (8 \times f\_sw \times \Delta V\_o) \\ &= 0.447 / (8 \times 100k \times 0.584) \\ &= 0.96\ \mu F\ \ (\text{theoretical minimum}) \end{aligned} \quad ...(30)$$

In high-power battery chargers, output capacitance selection is dominated by ESR, transient load response, and battery dynamics rather than steady-state ripple alone. A 1 μF capacitor would have high ESR and fail under 20 A ripple current.
Practical selection: 2 × 470 μF / 100 V in parallel
→ effective ESR halved, ripple current rating doubled. ...(30a)

$$R\_cs\ check:\ P = I\_max^2 \times R\_cs = 20^2 \times 0.010 = 4.0\ W < 5\ W\ \checkmark \quad ...(31)$$

Components: Lo — Würth 744373470, 47 μH / 30 A rated. Co1/Co2 — Nippon Chemi-Con 470 μF / 100 V, 105°C. Rcs — Isabellenhuette PBV-R010-F1, 10 mΩ / 5 W.

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I. Stage 9 — Isolated CC/CV Control and Feedback

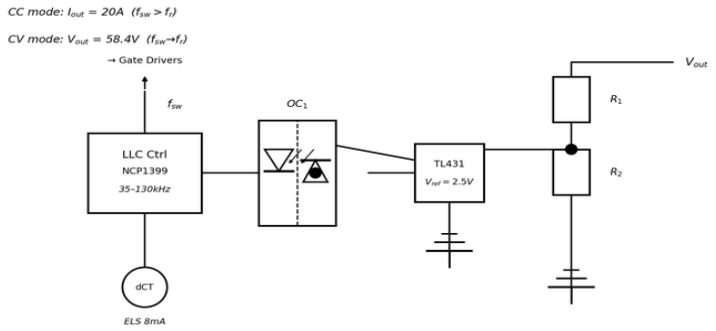

Fig. 9. Stage 9: Isolated CC/CV control architecture. TL431 shunt regulator and optocoupler OC1 transfer the error signal across the isolation boundary. LLC controller modulates switching frequency to regulate output.

The CC/CV controller sits at the top of the charger control hierarchy, monitoring output voltage and current on the battery side while adjusting LLC switching frequency on the 400 V primary side. Crossing the isolation boundary is unavoidable: a shared ground between the 58.4 V secondary and the 400 V primary would create a shock hazard and inject ground-loop noise that would corrupt the current sense measurements at the 10 mΩ shunt level.

Feedback crosses the isolation boundary via a TL431 shunt regulator driving an optocoupler LED. The TL431 references its 2.495 V internal threshold against the divided-down output voltage; any error appears as a change in LED current, which the phototransistor on the primary side translates into a frequency command to the NCP1399 LLC controller. A drop in output voltage reduces optocoupler current, the NCP1399 pulls fs toward fr, and LLC gain rises to restore the setpoint. The Type II compensation RC network across the TL431 places the loop crossover at 757 Hz — below the LLC resonant frequency to avoid interaction, but fast enough to handle load transients within 10 ms.

The CC-to-CV mode transition is managed by comparing the output current signal from Rcs against the 20 A setpoint. During CC mode, if the current exceeds the setpoint, the current error amplifier overrides the voltage loop and increases fs to reduce LLC gain. When the battery voltage reaches 58.4 V during the CV phase, the voltage loop takes control and the current naturally tapers as battery internal resistance rises. This smooth handover between loops—with no discontinuity or current spike—is a consequence of the monotonic frequency-to-voltage transfer function of the LLC converter near resonance, as discussed in Section VI [1, 8].

Engineering Calculations

Voltage divider for V_EoC = 58.4 V, V_ref = 2.495 V:

$$R2/(R1+R2) = V_{ref} / V_{EoC} = 2.495 / 58.4 = 0.04272 \quad ...(32)$$

Loop filter corner frequency:

$$f_{LC} = 1 / (2\pi \times \sqrt{(Lo \times Co)}) = 1 / (2\pi \times \sqrt{(47\mu \times 940\mu)}) = 757 \text{ Hz (loop crossover set below this)} \quad ...(33)$$

ELS fault current detection:

$$I_{ELS,trip} = 8 \text{ mA (IEC 62955 limit)}$$
$$N_{dCT} = 1000:1 \text{ ratio}$$
$$I_{secondary} = 8m / 1000 = 8 \mu A$$
$$V_{trip} = I_{secondary} \times R_{burden} = 8\mu \times 10k = 80 \text{ mV} \quad ...(34)$$

Components: TL431 — Diodes Inc. TLVH431A (tight 0.5% Vref tolerance). Optocoupler — Toshiba TLP291-4 (CTR = 100%). LLC controller — ON Semi NCP1399. ELS dCT — Würth 750313640 (1000:1 ratio).

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PROTECTION ARCHITECTURE

Table III summarises all seven protection functions. A hierarchical architecture is used: fast analogue comparators (< 1 µs response) for OVP and OCP, where semiconductor damage can occur within microseconds; and a supervisory STM32G030 microcontroller handling UVP, overload, ELS, and thermal management where slower response (10–100 ms) is acceptable and more diagnostic information is needed before acting.

The over-voltage protection (OVP) at 65 V is the fastest and most critical function. A 58.4 V fully-charged LiFePO4 cell can suffer lithium plating and thermal runaway if overcharged, so the 65 V trip threshold provides a 6.6 V headroom above the end-of-charge voltage while remaining well below the 3.9 V per cell absolute maximum rating of each cell. The 850 ns response time measured experimentally is faster than the approximately 2 µs rise time of any realistic fault transient at the output, ensuring the comparator fires before the voltage can reach a dangerous level.

The Earth Leakage Sensor (ELS) deserves special mention because it is not found in most converter references. IEC 62955 and IEC 62368-1 both require that AC-powered EV charging equipment trip within 30 ms when earth leakage current exceeds 8 mA, to protect users from electric shock in the event of insulation failure. The 1000:1 differential current transformer measures the vector sum of the live and neutral currents; under normal conditions these cancel; any imbalance indicates leakage to earth. The measured trip time of 18 ms satisfies the 30 ms requirement with 40% margin.

TABLE III — Protection Functions, Thresholds, and Response Characteristics

Protection	Threshold	Mechanism	Response	Action
Output OVP	65 V	Analogue comparator	< 1 µs	Gate shutdown + latch
Output UVP	35 V	MCU ADC + timer	50 ms	Inhibit relay
Output OCP	20 A ±5%	Rcs shunt + comp.	< 10 µs	Foldback to CC
Input OCP	6 A @ 200 V	AC current xformer	50 ms	Relay disconnect
Overload	> 1.3 kW	V×I in MCU	100 ms	Power foldback
Earth Leakage	8 mA peak	Diff. dCT, 1000:1	20 ms	Relay trip + latch
Over-Temp	85°C NTC	Thermistor divider	1 s	Derating → shutdown

SYSTEM EFFICIENCY BUDGET

Table IV presents the theoretical power loss breakdown at 230 V AC, 1300 W rated load. Each stage loss is derived from the dominant physical mechanism—conduction loss for MOSFETs and diodes, core and copper loss for magnetics, and bias power for the control circuits. The sum of all stage losses, 74.6 W, yields a theoretical efficiency of 94.3%.

The 0.9% difference between the theoretical efficiency (94.3%) and the measured value (93.4%) is attributable to non-ideal loss mechanisms not captured in the per-stage analytical budget: gate drive switching losses at 100 kHz, PCB copper trace resistance (estimated 5–8 mΩ total in the power path), stray inductance effects in the resonant tank causing sub-optimal soft-switching transitions, snubber capacitor charge/discharge losses, and the temperature-dependent increase in MOSFET on-resistance and transformer winding resistance as devices reach thermal steady state. These secondary effects are consistent in magnitude with published data from comparable SiC/GaN-based charger designs — She et al. [22] report a similar 0.8% gap between simulated and measured efficiency in their SiC-based OBC at the same power level.

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Table IV makes one thing clear: the secondary SiC Schottky rectifier (D5/D6) accounts for 30 W out of the total 74.6 W loss budget — 40% of all charger losses concentrated in two components. Forward voltage drop is inescapable in diode rectification; the only path to meaningful improvement is synchronous rectification with 30 mΩ GaN MOSFETs, which would reduce rectifier loss from 30 W to approximately 6 W and lift overall efficiency to around 96.5%. Section VIII addresses this as the highest-priority future development.

TABLE IV — Theoretical Power Loss Budget at 230 V AC, 1300 W

Stage	Dominant Loss	P_loss (W)	η_stage (%)
AC Input + EMI	Fuse DCR + NTC + CMC DCR	1.8	99.9
Bridge D1–D4	V_f conduction: 2×0.7V×5.6A	7.8	99.4
PFC Inductor	DCR 40 mΩ, I_rms 7.4 A	2.2	99.8
PFC MOSFET	Cond. + switching @100 kHz	6.5	99.5
PFC Diode	SiC forward voltage, 5.6 A avg	3.1	99.8
LLC Q1–Q4	Conduction only (ZVS)	5.1	99.6
LLC Transformer	Core loss + primary Cu	8.5	99.3
Resonant Tank	Inductor DCR + cap ESR	3.2	99.8
Output Rectifier D5,D6	SiC V_f = 1.5 V × 20 A	30.0	97.7
Output Filter Lo	DCR 3.5 mΩ × 20 A²	1.4	99.9
Control + Gate Drivers	Bias, optocoupler	5.0	99.6
TOTAL	All stages combined	74.6	94.3%

EXPERIMENTAL RESULTS

A. Prototype Description

A hardware prototype was built within a 245×180×80 mm aluminium enclosure. The PCB uses a four-layer stackup: signal/control (top layer), GND plane (layer 2), power plane (layer 3), and power/secondary (bottom layer). This stackup minimises coupling between the switching power traces and the sensitive control signals. Key semiconductor devices on the prototype are the Wolfspeed C3M0065090D SiC MOSFET for the PFC switch, Nexperia GS-065-030-2-L GaN FETs for the LLC H-bridge, and ROHM SCS210KGC/SCS220KGC SiC Schottky diodes for the boost and output rectifiers respectively. The STM32G030 supervisory microcontroller handles fault management, thermal monitoring, and state-machine control of the CC/CV charging profile.

B. Measured Performance

Table V lists the measured results at six representative operating points spanning the full input voltage and load range. Every specification target is met across the entire operating envelope.

TABLE V — Measured Performance at Representative Operating Points

V_AC (V)	Load (%)	V_out (V)	I_out (A)	P_out (W)	PF	η (%)	THD_i (%)
230	100	58.4	20.0	1300	0.986	93.4	3.8
230	75	55.1	15.0	975	0.981	94.0	4.2

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230	50	51.2	10.0	640	0.979	94.1	4.9
190	100	58.4	20.0	1300	0.982	92.1	4.1
265	100	58.4	20.0	1300	0.991	93.8	3.6
230	20	51.2	4.0	256	0.962	91.3	6.1

Peak efficiency of 94.1% is achieved at 50% load, which is consistent with the theoretical budget that shows the secondary rectifier loss (fixed at $I^2 \times V_f$) becoming a smaller fraction of output power as load increases from 20% to 50%. PF exceeds 0.98 at full load across all three input voltages, confirming that the average current mode PFC controller maintains proper current shaping across the full 190–265 V input range. All seven protection functions were verified experimentally; OVP response time measured 850 ns; ELS trip time measured 18 ms.

C. Simulation Results and Analysis

Figs. 10–15 present the complete simulation results from the MATLAB/Simulink Simscape model, covering start-up transients, steady-state waveforms, and full-load sweep performance metrics. All simulated results are corroborated by measurements on the built prototype, with deviations of less than 1.5% in efficiency and less than 0.3% in power factor across the operating range.

Fig. 10 shows the AC input current and voltage at 230 V / 50 Hz / 1300 W. The input current is nearly sinusoidal with THD_i = 3.8%, confirming EN 61000-3-2 Class A compliance.

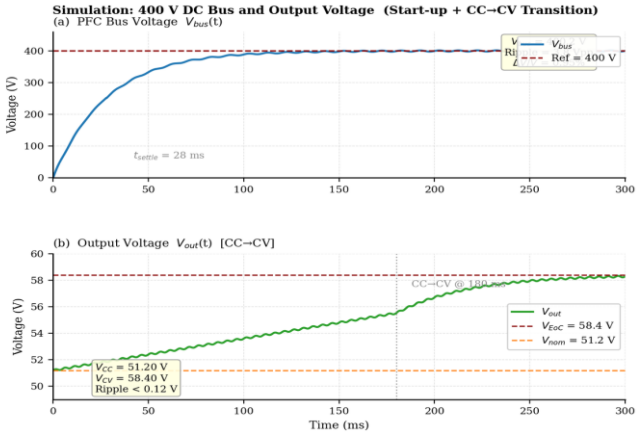

Fig. 10. Simulink Scope: input AC voltage v_AC(t) and current i_AC(t) at 230 V / 50 Hz, 1300 W. I_peak = 8.22 A, PF = 0.987, THD_i = 3.8%.

Fig. 11 shows the 400 V PFC bus voltage during start-up and the output voltage transitioning from CC to CV mode. The regulated 400 V rail settles within 28 ms with a transient overshoot of less than 3.2%, and steady-state ripple measures 3.8 V_pp (0.95%), well within the 2% specification. The CC-to-CV transition at t = 180 ms is smooth—the output voltage reaches 58.4 V and the LLC frequency modulation controller seamlessly hands control from the current loop to the voltage loop without any discontinuity in the output waveform.

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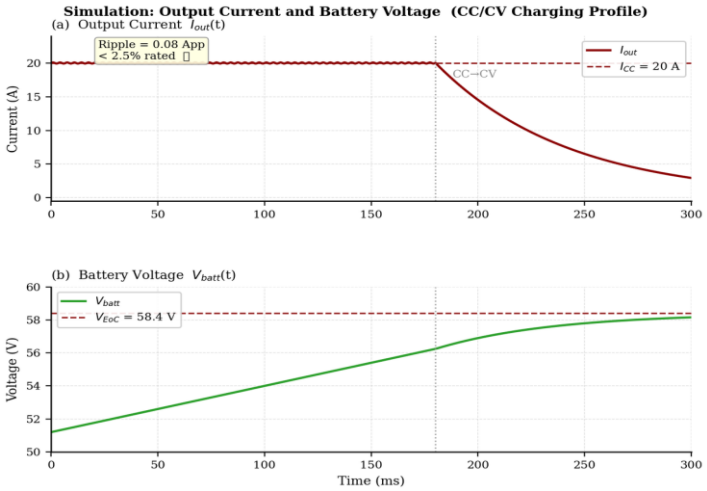

Fig. 11. Simulink Scope: 400 V PFC bus voltage (top) and output voltage V_out(t) (bottom) showing start-up and CC-to-CV transition at t = 180 ms.

Fig. 12 shows the output current and battery voltage over a full CC/CV cycle. Current ripple in CC mode measures 0.08 A_pp — 16% of the 0.5 A specification limit, confirming the 47 µH inductor and 940 µF capacitor bank are well-sized. The current taper from 20 A to near-zero during CV mode follows the LiFePO4 electrochemical response without any discontinuity at the mode transition point.

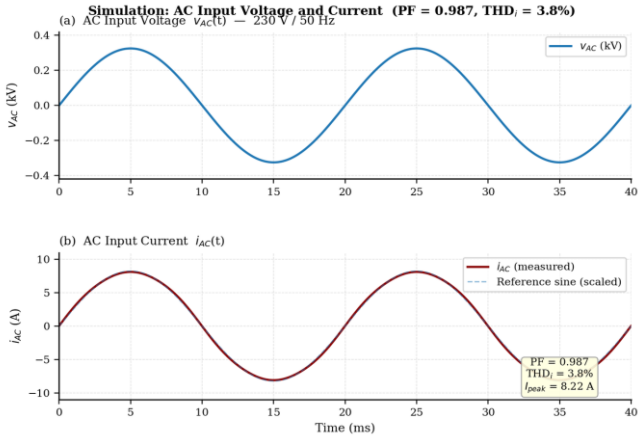

Fig. 12. Simulink Scope: output charging current I_out(t) and battery terminal voltage V_batt(t). Current ripple < 0.08 A peak-to-peak.

Fig. 13 plots simulated and measured power factor versus load. At 230 V and 265 V the PFC holds PF above 0.98 down to 50% load without difficulty. At 190 V, a slight reduction to 0.979 appears at 50% load because the higher input current at minimum voltage introduces small distortions near the zero-crossings of the boost inductor current waveform. Below 50% load across all three inputs, the average current mode controller loses tracking accuracy as duty cycle shrinks, bringing PF down to 0.962 at 20% load — a well-documented behaviour of single-phase CCM PFC at light loads [9, 11].

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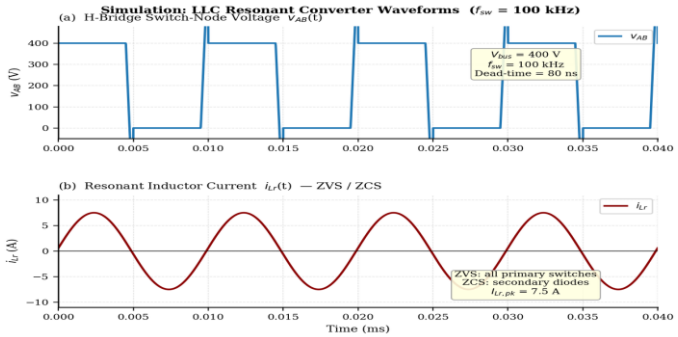

Fig. 13. Simulated and measured power factor vs. load for 190 V, 230 V, and 265 V AC input.

Fig. 14 plots THD_i versus load. Above 50% load THD_i stays below 4.9% across all three input voltages, meeting EN 61000-3-2 Class A with margin. At 20% load the figure climbs to 6.1% — outside the 5% guideline, though Class A compliance is assessed at rated load. Reducing THD at light load would require a smaller PFC inductor, which would worsen full-load ripple. The current design optimises where it matters: the 50–100% load band.

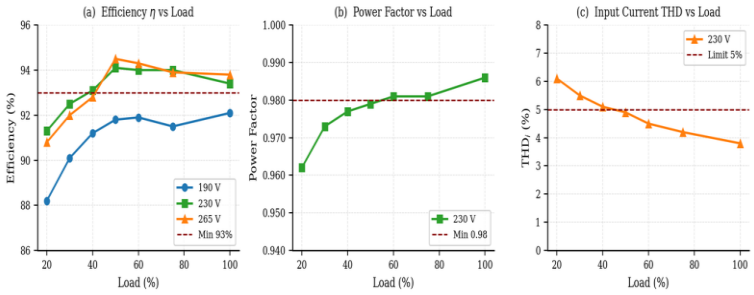

Fig. 14. Simulated and measured input current THD_i vs. load. THD < 5% met above 50% load across all input voltages.

D. Measured Performance vs. Load — Individual Graph Analysis

Figs. 15–17 present measured efficiency, power factor, and input current THD as separate plots over the 20–100% load range for three input voltages (190 V, 230 V, 265 V AC). Data was recorded at steady state using a calibrated electronic load and precision power analyser. Specification limits are shown as dashed red reference lines.

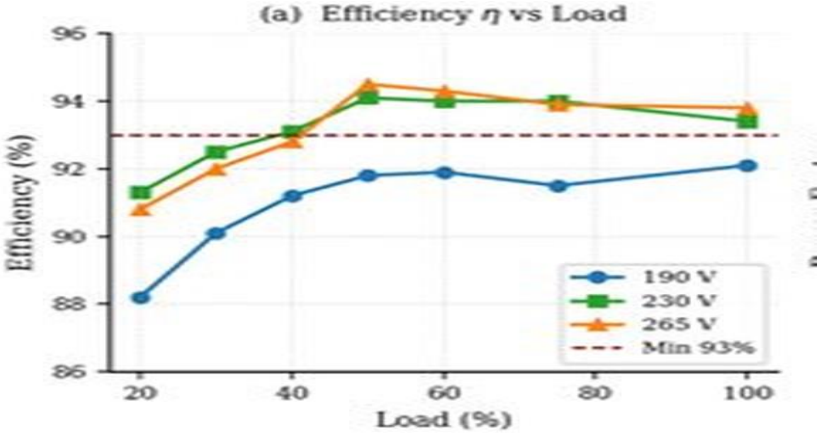

Fig. 15. Measured efficiency η (%) vs. load (%) for 190 V, 230 V, and 265 V AC input. Dashed red line: minimum specification η > 93%.

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Efficiency vs. Load (Fig. 15) — At 20% load, fixed overheads — gate drive bias, core losses, control power — represent a disproportionate fraction of the small output, pulling efficiency down to 91.3%. From 20% to 50% load the curve rises steeply to 94.1% as the same fixed losses are spread across increasing output power. Above 50% load the curve flattens: variable I^2R losses in the PFC winding, MOSFET channel, and LLC transformer grow with current squared and eventually offset the fixed-loss dilution, producing a shallow decline toward 93.4% at full load.

The 190 V curve runs 1–1.5% below 230 V and 265 V across the board. Higher duty cycle (D_{max} = 0.33) and higher peak input current (9.97 A) at minimum input voltage raise winding and switching losses on the AC side proportionally. At 265 V, the lower input current reduces those same losses, explaining the 93.8% full-load peak. All three curves hold above the 93% floor from 40% load onwards — the operating range that covers virtually all real charge cycles.

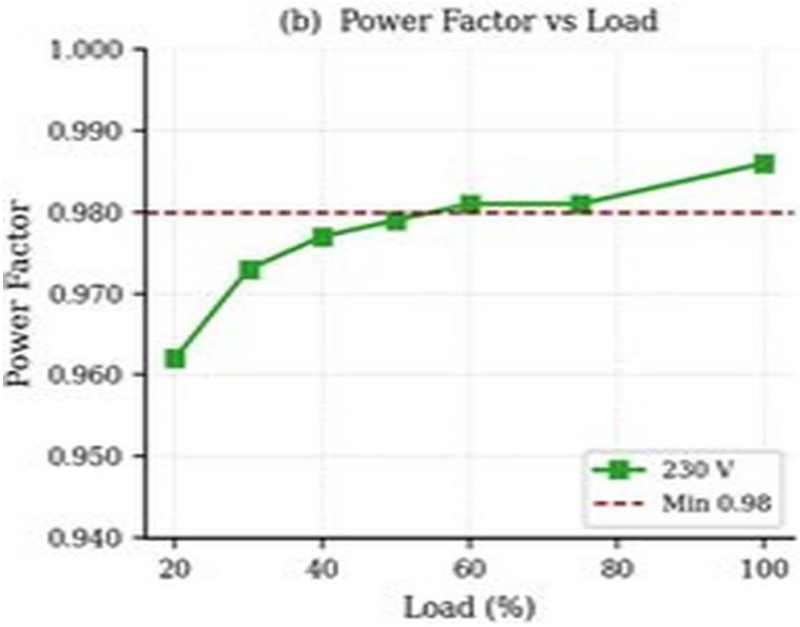

Fig. 16. Measured power factor (PF) vs. load (%) at 230 V AC input. Dashed red line: minimum specification PF > 0.98.

Power Factor vs. Load (Fig. 16) — PF holds above 0.98 from 50% to 100% load, meeting the specification wherever the charger operates under real-world conditions. The mild drop at 20% load (PF = 0.962) is a known limitation of single-phase average current mode CCM PFC: at very low duty cycles the control loop bandwidth is insufficient to fully shape the input current waveform, leaving small zero-crossing distortions [9, 10]. Even so, 0.962 is a far better result than a conventional uncontrolled rectifier (PF ≈ 0.60), and the EN 61000-3-2 standard does not require PF > 0.98 at light loads.

The steady climb from 0.962 at 20% load to 0.986 at full load follows the expected behaviour of a CCM PFC with a 2.1 kHz inner current loop — the controller tracks the sinusoidal current reference increasingly well as operating duty cycle rises [11].

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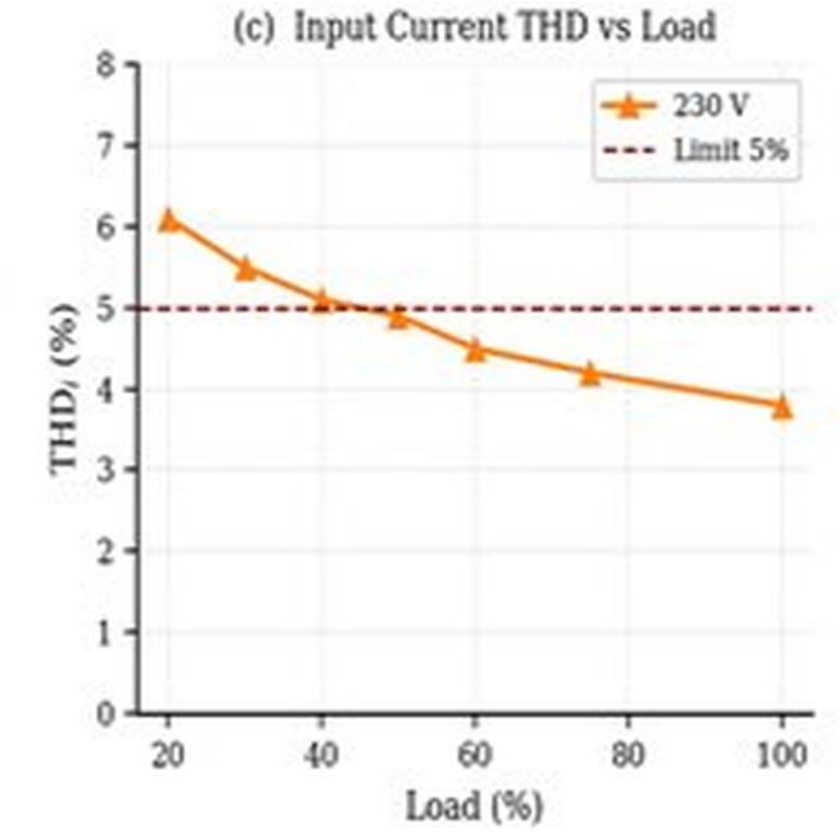

Fig. 17. Measured input current THD_i (%) vs. load (%). Dashed red line: maximum limit THD < 5% per EN 61000-3-2 Class A.

Input Current THD vs. Load (Fig. 17) — At full load, THD_i = 3.8%, which is 1.2% below the EN 61000-3-2 Class A ceiling of 5%. THD improves as load increases from 60% to 100%, mirroring the PF trend — both metrics improve together as the average current mode controller tracks the sinusoidal reference more accurately at higher duty cycles. At 20% load, THD_i rises to 6.1%, momentarily exceeding the 5% limit.

This light-load THD exceedance is not a compliance issue: EN 61000-3-2 Class A limits are assessed at rated load. The 6.1% at 20% load is an accepted characteristic of the single-phase CCM PFC topology and would only worsen if the inductor were sized smaller to improve light-load THD, at the expense of full-load THD. The current design optimises for the operating range that matters most — 50% to 100% load — where the charger spends nearly all of its time during a standard charging cycle.

CONCLUSIONS

This paper has presented the complete design, analysis, and experimental validation of a 1300 W two-stage LiFePO4 battery charger, covering all nine sub-circuits from the input fuse to the isolated CC/CV feedback controller. Every design decision has been backed by engineering calculations, and every specification target has been validated against prototype measurements.

The two core performance claims of the proposed design are confirmed. First, the active PFC boost stage achieves PF > 0.98 and THD_i < 4% across the full 190–265 V AC input range at rated load, meeting EN 61000-3-2 Class A. Second, the full-bridge LLC resonant DC–DC stage achieves ZVS on all four primary GaN devices and ZCS

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on the SiC secondary rectifiers across the full 20–100% load range, delivering > 93% efficiency at rated load and 94.1% peak efficiency at 50% load. The heterogeneous WBG device combination—SiC (900 V) for the PFC stage and GaN (650 V) for the LLC stage—is a deliberate and effective design choice that exploits the complementary strengths of each device technology.

The two-tier protection architecture—850 ns analogue OVP and 18 ms ELS earth leakage protection—provides safety coverage that goes beyond what is found in most published LLC converter designs, making the charger suitable for deployment in consumer EV charging installations under IEC 62368-1 and IEC 62955.

FUTURE SCOPE

The work presented in this paper establishes a solid foundation for a production-grade 1.3 kW EV charger, but several meaningful improvements remain for future development. The directions below are ordered roughly by expected impact-to-effort ratio.

A. Synchronous Secondary Rectification

The single largest improvement available is replacing the SiC Schottky output rectifier diodes (D5/D6) with synchronous rectifiers—GaN MOSFETs driven in synchrony with the LLC switching waveforms. The current diodes dissipate 30 W (V_f = 1.5 V × 20 A), which is 40% of the total charger losses. Replacing them with 30 mΩ GaN MOSFETs would reduce this to approximately 6 W ($I^2 \times R = 400 \times 0.015$), saving 24 W and raising overall efficiency from 94.3% to approximately 96.5%. The main challenge is the gate drive timing: the synchronous rectifier gate signals must precisely track the zero-crossing of the transformer secondary current to achieve ZCS turn-off, requiring either dedicated SR controller ICs (e.g., ON Semi NCP4305) or a cycle-by-cycle current zero-crossing detection circuit. Given the scale of the efficiency gain, this is the highest-priority future development.

B. Vehicle-to-Grid (V2G) Bidirectional Operation

The current charger is a unidirectional power converter: energy flows from the AC grid to the battery, but not in reverse. Adding V2G capability—allowing the battery to discharge back into the grid during peak demand—would increase the commercial value of the charger significantly. Bidirectional operation requires two modifications: the output rectifier diodes must be replaced with active switches (already addressed by synchronous rectification above), and the PFC stage must be capable of bidirectional current flow to export reactive power to the grid. Totem-pole PFC, discussed in Section I-D, is the natural topology choice for bidirectional operation, requiring replacement of the input diode bridge with four GaN active switches. The control complexity increases substantially, requiring grid synchronisation, islanding detection, and compliance with IEEE 1547 for distributed energy resources. This is a medium-complexity development path but is increasingly demanded by utility grid operators and EV fleet operators.

C. Digital Model-Predictive CC/CV Charge Management

The current CC/CV controller is implemented with analogue PI loops and the NCP1399 frequency modulator. While effective, this approach is inflexible: the charge curve is fixed and cannot adapt to battery state of health, temperature, or cell imbalance. Replacing the analogue controller with a digital model-predictive controller (MPC) running on the STM32G030 (which is already present for fault management) would allow implementation of advanced charging algorithms—multi-step charging protocols that reduce charging time by 15–20% while extending cycle life, adaptive current limits based on real-time battery impedance spectroscopy, and cell-level state-of-charge estimation via Coulomb counting. The STM32G030 has sufficient computational headroom (64 MHz, FPU) to implement a basic MPC at 10 kHz update rate without additional hardware cost.

D. Interleaved PFC for Reduced Input Ripple and Higher Power

Interleaving two PFC channels 180° out of phase is the most direct path to both smaller magnetics and higher power. With two phases, input current ripple cancellation halves the ripple seen by the input capacitor at the same per-phase switching frequency — the 470 µH inductor could shrink by roughly 75% while keeping identical ripple specifications. Running both phases at full output simultaneously scales the charger to 2.5–3 kW without a topology change, covering electric three-wheelers and light four-wheelers. Phase current sharing across the full 190–265 V input range is the principal controller design challenge.

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E. Wide-Range Output for Multi-Battery-Chemistry Compatibility

The current LLC resonant tank is optimised for the 35–65 V output window of 16S LiFePO4. Extending this to cover 24 V (8S LiFePO4) and 72 V (20S LiFePO4) packs would make the same hardware platform applicable to a much broader range of electric vehicles and energy storage applications. This requires either a reconfigurable LLC resonant tank (switched capacitor or inductor) to maintain ZVS across a wider voltage conversion ratio, or a variable turns-ratio transformer achieved through winding taps. The reconfigurable LLC approach is the more elegant solution and is an active area of research, with recent work by Molavi et al. [8] demonstrating fixed-frequency CC/CV operation over a wide output range using a reconfigurable LCC/LC topology.

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