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# DESIGN AND IMPLEMENTATION OF A LOW-POWER FULL ADDER IN NANOMETER CMOS TECHNOLOGY FOR DIGITAL PROCESSOR APPLICATIONS

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***ABSTRACT*:**

The growing demand for low-power integrated circuits in nanometer technologies has made power reduction in digital arithmetic units a fundamental design challenge. The full adder, as the most elementary building block of arithmetic logic units and digital processors, plays a central role in determining the energy efficiency of the entire processing system. This study aimed to design, implement, and evaluate a low-power one-bit full adder in nanometer CMOS technology for digital processor applications. Two implementations were simulated using Cadence Virtuoso in the ADE L environment, employing the 90 nm GPDK process at a supply voltage of 1.8 V and an operating temperature of 27°C. The first design was based on standard CMOS logic comprising 36 transistors, and the second was based on the modified gate diffusion input technique comprising 20 transistors. Performance evaluation was conducted based on average power consumption, propagation delay, power-delay product, and occupied area. The results demonstrated that the MGDI design achieved a 61.6% reduction in average power consumption and a 79.6% improvement in propagation delay relative to the standard CMOS implementation. The power-delay product decreased by 92.2%, while transistor count and occupied area were reduced by 44.4% and 51.1%, respectively. Functional correctness was verified across all eight possible input combinations for both designs. These findings indicate that the MGDI technique constitutes an effective approach for low-power full adder design in nanometer CMOS technology and represents a suitable candidate for energy-efficient digital processor applications.

***Keywords**: CMOS technology, full adder, low-power design, MGDI, propagation delay.*

## INTRODUCTION

The electronics industry has witnessed remarkable growth over the past few decades [1]. Very large-scale integration (VLSI) technology has emerged as one of the fundamental pillars driving this advancement [2]. By enabling the integration of millions of transistors onto a single chip, VLSI has fundamentally transformed the landscape of modern semiconductor design [3]. VLSI circuits form the backbone of microprocessors, memory devices, and complex digital integrated systems [4]. In VLSI design, speed, area, and power consumption are the three parameters of paramount importance [5]. As transistor density continues to increase, power management has become one of the most critical challenges confronting circuit designers [6]. The simultaneous optimization of these three parameters in modern digital systems is therefore an indispensable requirement [7]. Since the performance of fundamental arithmetic operations is directly governed by these parameters, their improvement translates into enhanced overall system efficiency. The full adder is the most elementary arithmetic unit in digital circuits, responsible for performing binary addition [8]. It consists of three inputs, namely A, B, and Cin, and produces two outputs, Sum and Cout [9]. As the primary building block for more complex arithmetic circuits, the full adder plays an integral role in digital circuit hierarchies [10]. It serves as the core computational element within arithmetic logic units (ALUs) and digital processors [11]. Beyond ALUs, full adders are extensively employed in multipliers, digital filters, and digital signal processing (DSP) units [12]. Since full adder cells reside on many critical paths of a system, their propagation delay and power dissipation directly impact the overall performance of the processing unit [13]. Reducing the power consumption of full adders without compromising operating speed remains a primary objective for VLSI designers [14]. Consequently, the design of low-power full adders in nanometer-scale technology holds significant importance for modern digital systems. The continuous


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scaling of CMOS technology has reduced transistor dimensions from 90 nm to 28 nm and below [15]. Although dimensional scaling has improved circuit speed, it has simultaneously introduced severe power-related challenges [16]. As device dimensions shrink, short-channel effects become increasingly pronounced, degrading transistor behavior [17]. Leakage current rises significantly as transistor dimensions are reduced to the nanometer regime [18]. This leakage persists even in standby mode, resulting in considerable static power dissipation [19]. Dynamic power, arising from the charging and discharging of load capacitances, also constitutes a substantial fraction of total power consumption at high operating frequencies [20]. Collectively, both static and dynamic power components contribute significantly to the overall power budget in nanoscale designs [21]. The growing demand from Internet of Things (IoT) applications, portable devices, and wearable systems further necessitates the development of ultra-low-power circuits [22]. It is therefore imperative to systematically investigate and compare various logic styles capable of addressing these power challenges. Several logic styles and design techniques have been proposed for the implementation of low-power full adders [23]. Among them, hybrid full adder topologies have demonstrated competitive performance in terms of transistor count and power efficiency [24]. The gate diffusion input (GDI) technique reduces circuit complexity by minimizing the number of required transistors [25]. Graphene nanoribbon field-effect transistor (GNRFET)-based implementations have also been explored as emerging alternatives for low-power design [26]. Pass transistor logic (PTL) offers notable advantages in reducing propagation delay and switching power [27]. Approximate computing approaches have been investigated for applications tolerant of minor computational errors [28]. Adiabatic logic techniques recover energy from load capacitances and have shown promise in further reducing dynamic power dissipation [29]. Ternary logic implementations using multi-threshold transistors have been examined for efficient digital computing architectures [30]. Furthermore, carbon nanotube field-effect transistor (CNTFET)-based full adders have been studied for their applicability in digital signal processing systems [31]. A comprehensive and fair comparison of these diverse approaches under identical simulation conditions remains an unresolved necessity in the literature. Considerable research effort has been directed toward the design of low-power full adders in nanometer CMOS technology [32][33]. Ahmadi et al. (2023) investigated energy-efficient approximate full adder designs for error-tolerant applications and demonstrated that their proposed circuit achieves a significant reduction in power consumption compared to conventional CMOS implementations [34]. Nirmalraj et al. (2023) examined a ten-transistor full adder based on the GDI technique for energy-efficient arithmetic applications and reported considerable improvements in both power dissipation and propagation delay relative to standard CMOS designs [35]. Despite these contributions, a comprehensive comparative study simultaneously evaluating power consumption, propagation delay, and power-delay product (PDP) of low-power full adder designs in nanometer CMOS technology for digital processor applications remains largely absent from the literature. This gap underscores the need for a systematic and unified evaluation framework to assess these performance metrics under consistent simulation conditions. This study aims to design and implement low-power full adder circuits in nanometer CMOS technology and evaluate their performance in terms of power consumption, propagation delay, and power-delay product (PDP) for digital processor applications. It is hypothesized that the application of targeted optimization techniques in nanometer CMOS design can substantially reduce full adder power consumption without significant degradation in operating speed or functional accuracy. To the best of the authors' knowledge, this is the first study to conduct a comprehensive comparative analysis of multiple logic styles under identical simulation conditions in nanometer CMOS technology, with simultaneous evaluation of power, delay, and PDP metrics in the specific context of digital processor applications. The subsequent sections address the design methodology and simulation setup, followed by an analysis of the simulation results and performance evaluation.

## DESIGN METHODOLOGY

### 2.1 Full Adder Circuit Design and Implementation

A one-bit full adder is a combinational circuit that performs the binary addition of two input bits, A and B, along with a carry-in signal, Cin. The circuit produces two outputs: Sum, which represents the addition result, and Cout, which carries the overflow to the next significant bit. The Boolean expressions governing the logical behavior of this circuit are given in equations (1) and (2).

$$\text{Sum} = \boldsymbol{A} \oplus \boldsymbol{B} \oplus \boldsymbol{C_{in}} \tag{1}$$

$$\boldsymbol{C_{out}} = \boldsymbol{AB} + (\boldsymbol{A} \oplus \boldsymbol{B}) \cdot \boldsymbol{C_{in}} \tag{2}$$

In equation (1), the symbol $\oplus$ denotes the exclusive-OR (XOR) operation. The Sum output assumes a logic-high value when an odd number of inputs are simultaneously at logic one. In equation (2), Cout becomes logic one


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under two conditions: when both A and B are simultaneously at logic one, or when the XOR of A and B and the carry-in Cin are both at logic one. The complete truth table of the full adder, covering all eight possible input combinations and their corresponding outputs, is presented in Table 1.

Table 1. Truth table of the one-bit full adder.

| A | B | Cin | Sum | Cout |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

The circuit implementation adopted in this study is based on a cascaded XOR-NAND architecture. In this configuration, two XOR gates are employed in sequence to generate the Sum output, while two NAND gates are used to produce the Cout output. This underlying architecture is common to both the standard CMOS and MGDI implementations presented in this work; however, the transistor count, power dissipation characteristics, and overall performance differ substantially between the two approaches.

### 2.2 Proposed Circuit Topologies

#### 2.2.1 Standard CMOS Implementation

Complementary metal-oxide-semiconductor (CMOS) technology is the most widely adopted fabrication process for digital integrated circuits. In this technology, each logic gate is constructed from two complementary transistor networks. The pull-up network (PUN), formed by PMOS transistors, establishes a logic-one level at the output, while the pull-down network (PDN), formed by NMOS transistors, establishes a logic-zero level. These two networks operate in a complementary fashion such that, for any given input combination, exactly one network is in the conducting state while the other remains off.

In the standard CMOS implementation of the full adder, each XOR gate is composed of six PMOS transistors arranged in the pull-up network and six NMOS transistors forming the pull-down network. The NAND gates employed for Cout generation each consist of two PMOS transistors connected in parallel within the pull-up network and two NMOS transistors connected in series within the pull-down network. Consequently, the complete standard CMOS full adder circuit comprises 36 transistors in total, of which 18 are PMOS and 18 are NMOS. The width-to-length ratio (W/L) is set to 120/100 for both NMOS and PMOS transistors throughout all simulations. The full transistor-level schematic of this implementation is illustrated in Figure 1.

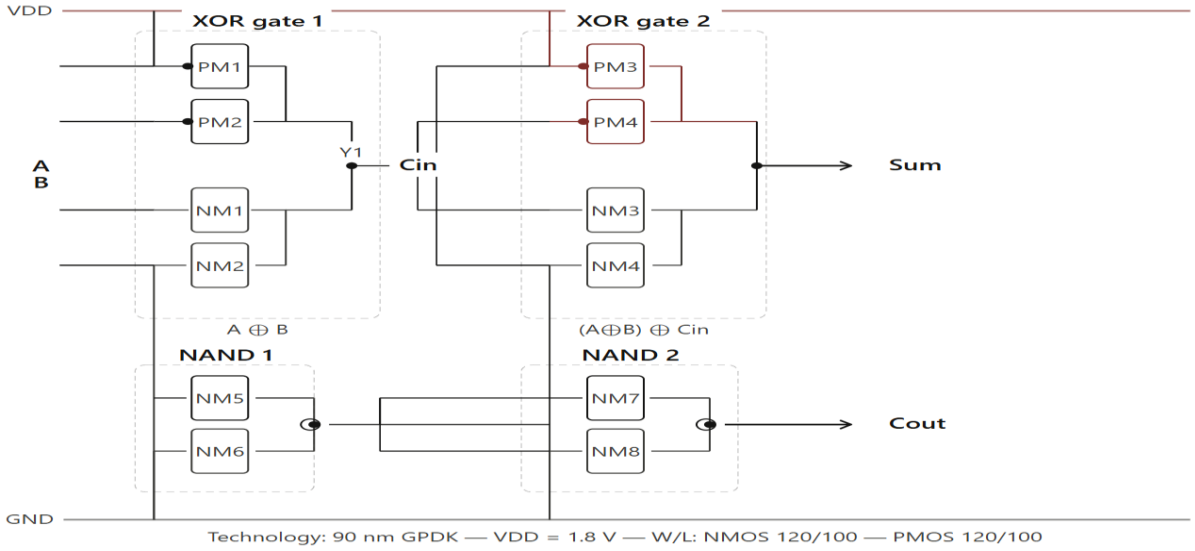


**Figure 1. Transistor-level schematic of the one-bit full adder based on standard CMOS logic — 90 nm GPDK technology, VDD = 1.8 V.**


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### 2.2.2 MGDI-Based Low-Power Implementation

The modified gate diffusion input (MGDI) technique is an efficient design methodology for realizing low-power, area-efficient digital logic circuits. In this technique, each fundamental cell consists of only two transistors, one PMOS and one NMOS, making it inherently compact. The MGDI cell has three input terminals: terminal G, which is connected to the gate of both transistors; terminal P, which is connected to the source of the PMOS transistor; and terminal N, which is connected to the source of the NMOS transistor. The output is taken from the common drain node of both transistors. The key distinction between the MGDI technique and its predecessor, the basic GDI technique, lies in the substrate connections. In MGDI, the bulk terminals of the NMOS and PMOS transistors are tied to ground and VDD, respectively, which ensures full compatibility with standard twin-well CMOS fabrication processes. The structure of the MGDI cell is illustrated in Figure 2.

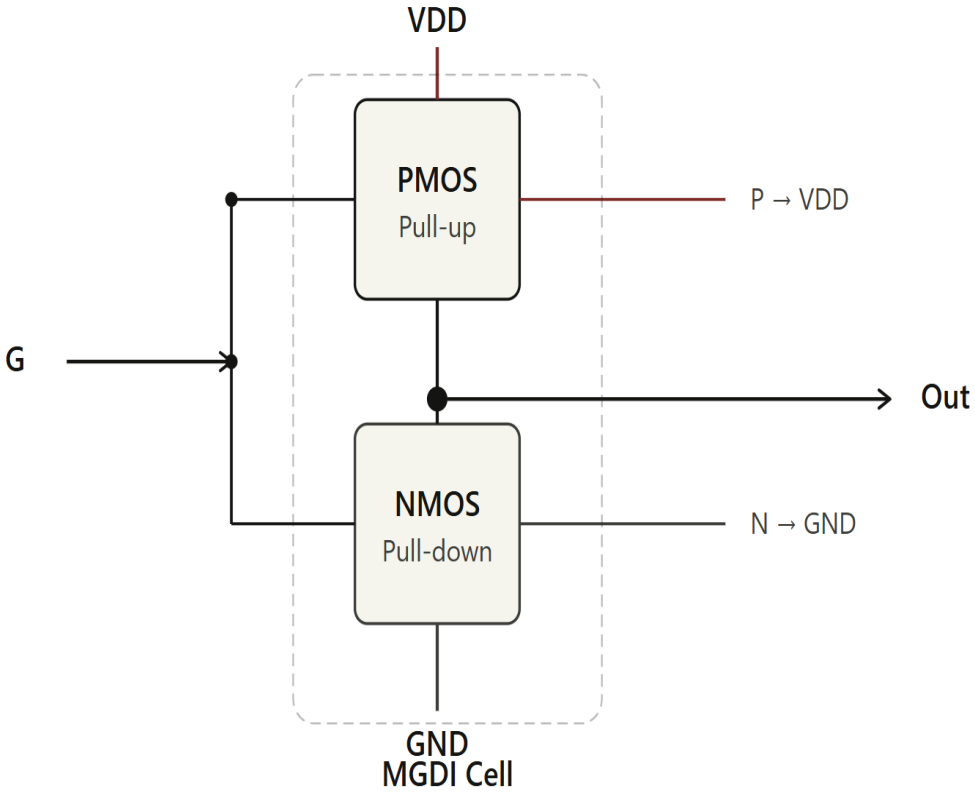


**Figure 2. Transistor-level structure of the Modified Gate Diffusion Input (MGDI) cell.**

By appropriately configuring the G, P, and N input terminals, the MGDI cell can implement a wide range of logic functions, including XOR, XNOR, AND, and OR, using only two transistors. This property enables the realization of complex logic circuits with a significantly reduced transistor count compared to standard CMOS implementations. In the MGDI-based full adder design, each XOR gate is realized using two PMOS and two NMOS transistors, and each NAND gate similarly employs two PMOS and two NMOS transistors. As a result, the complete MGDI full adder circuit contains 20 transistors in total, comprising 10 PMOS and 10 NMOS devices. This represents a 44.4% reduction in transistor count relative to the 36-transistor standard CMOS implementation. The transistor-level schematic of the MGDI full adder is presented in Figure 3.


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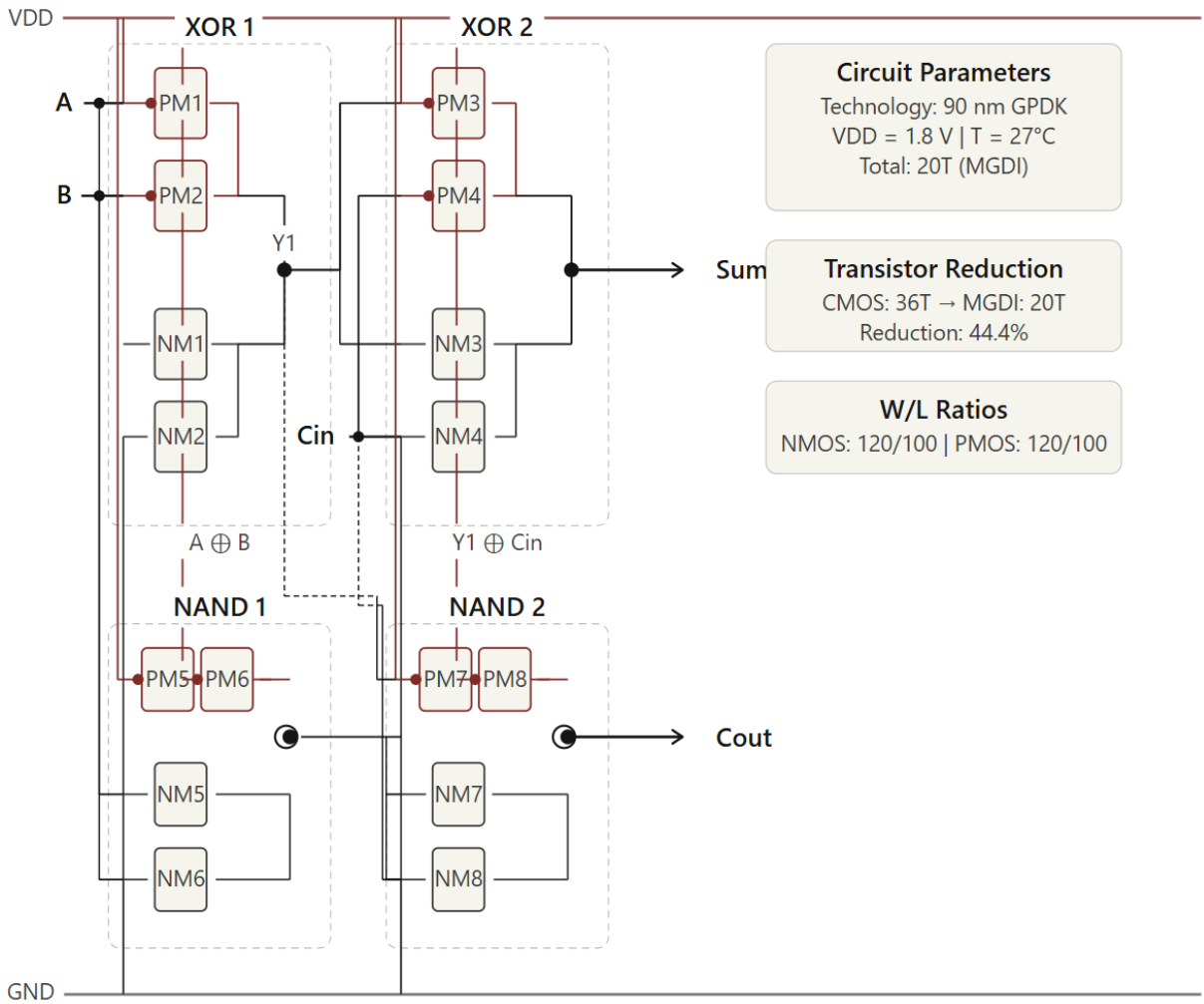


**Figure 3. Transistor-level schematic of the one-bit full adder based on the MGDI technique — 90 nm GPDK technology, VDD = 1.8 V.**

### 2.3 Power Dissipation Analysis in Nanometer CMOS Technology

The total power consumption of a CMOS circuit in the nanometer regime consists of two primary components. The first is dynamic power, which is dissipated during switching activity as load capacitances are alternately charged and discharged. This component is expressed by equation (3).

$$P_{dynamic} = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f \tag{3}$$

In equation (3), α is the switching activity factor, which represents the probability of an output transition occurring per clock cycle. $C_L$ denotes the total load capacitance at the output node in farads, $V_{DD}$ is the supply voltage in volts, and f is the operating frequency in hertz. In the MGDI-based implementation, the 44.4% reduction in transistor count leads to a proportional decrease in parasitic capacitances, thereby reducing $C_L$ and consequently lowering the dynamic power dissipation.

The second component is static power, which flows continuously regardless of circuit activity and originates primarily from subthreshold leakage currents through the transistors. This component is given by equation (4).

$$P_{static} = I_{leakage} \cdot V_{DD} \tag{4}$$

In equation (4), I_leakage represents the total leakage current flowing through all transistors in the circuit in amperes, and $V_{DD}$ is the supply voltage in volts. In 90 nm CMOS technology, transistor scaling significantly


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exacerbates leakage currents, making static power a non-negligible fraction of total power consumption. By reducing the number of transistors, the MGDI technique decreases the number of leakage paths, thereby contributing to a reduction in static power as well. The total power consumed by the circuit is the sum of both components, as expressed in equation (5).

$$P_{total} = P_{dynamic} + P_{static} \tag{5}$$

In equation (5), $P_{total}$ is the total power dissipation under normal operating conditions. The simultaneous reduction of both dynamic and static power in the MGDI design represents its primary advantage over standard CMOS for low-power digital processor applications.

**2.4 Simulation Environment and Parameters**

All simulations in this study were performed using Cadence Virtuoso in the Analog Design Environment L (ADE L) framework, which provides high-accuracy transistor-level circuit analysis. The technology employed is the standard Generic Process Design Kit (GPDK) at the 90 nm technology node. All circuits were simulated at a supply voltage of 1.8 V and an operating temperature of 27°C. The threshold voltage was set to 0.9 V for all designs, representing the point beyond which supply voltage increments lead to a significant increase in circuit current and power. A simulation stop time of 200 ns was selected to ensure complete coverage of all eight possible input combinations. A comprehensive summary of the simulation parameters is provided in Table 2.

**Table 2. Simulation parameters.**

| Parameter | Value |
|---|---|
| Simulation Tool | Cadence Virtuoso (ADE L) |
| Technology Node | 90 nm GPDK |
| Supply Voltage (V_DD) | 1.8 V |
| Threshold Voltage | 0.9 V |
| Operating Temperature | 27°C |
| Simulation Stop Time | 200 ns |
| NMOS W/L Ratio | 120/100 |
| PMOS W/L Ratio | 120/100 |
| Standard CMOS Transistor Count | 36 (18 PMOS + 18 NMOS) |
| MGDI Transistor Count | 20 (10 PMOS + 10 NMOS) |

**2.5 Performance Evaluation Metrics**

Three performance metrics were employed in this study to enable a quantitative comparison between the standard CMOS and MGDI full adder implementations. The first metric is propagation delay, which measures the time required for a logic transition to propagate from the input to the output of the circuit. This delay is calculated according to equation (6).

$$t_{pd} = \frac{t_{pHL} + t_{pLH}}{2} \tag{6}$$

In equation (6), $t_{pHL}$ denotes the propagation delay associated with a high-to-low output transition, and t_pLH denotes the delay corresponding to a low-to-high output transition. Both quantities are expressed in picoseconds, and their arithmetic mean is taken as the overall propagation delay of the circuit.

The second metric is average power consumption, which is extracted from transient simulation results within the ADE L environment and reported in microwatts. The third and most comprehensive metric is the power-delay product (PDP), which serves as a combined figure of merit for simultaneously assessing power efficiency and operating speed. The PDP is computed according to equation (7).

$$PDP = P_{avg} \times t_{pd} \tag{7}$$

In equation (7), $P_{avg}$ is the average power consumption of the circuit in watts and $t_{pd}$ is the propagation delay in seconds. The resulting product is expressed in joules. A lower PDP value indicates superior circuit performance in terms of the simultaneous optimization of power dissipation and speed, and a design achieving a lower PDP is considered more suitable for low-power digital processor applications.


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## RESULTS AND DISCUSSION

The simulation results of two one-bit full adder implementations based on standard CMOS and the MGDI technique are presented in this section. All simulations were performed using Cadence Virtuoso in the ADE L environment employing the 90 nm GPDK technology. A supply voltage of 1.8 V, an operating temperature of 27°C, and a simulation stop time of 200 ns were maintained identically for both designs. Performance evaluation was carried out based on power consumption, propagation delay, power-delay product, and occupied area.

### 4.1 Functional Verification

The logical correctness of the standard CMOS full adder was verified through transient simulation in the ADE L environment. All eight possible input combinations were applied sequentially over the 200 ns simulation window. The Sum output correctly assumed a logic-one value whenever an odd number of inputs were simultaneously at logic one. The Cout output correctly assumed logic one whenever two or three inputs were simultaneously active. The resulting waveform exhibits complete agreement with the truth table presented in the Methods section, and no logical errors were observed. The propagation delay of the standard CMOS circuit was extracted from signal transition analysis at the Sum output and measured at 28.971 ps. Figure 4 illustrates the output timing waveform of this implementation across the full simulation period.

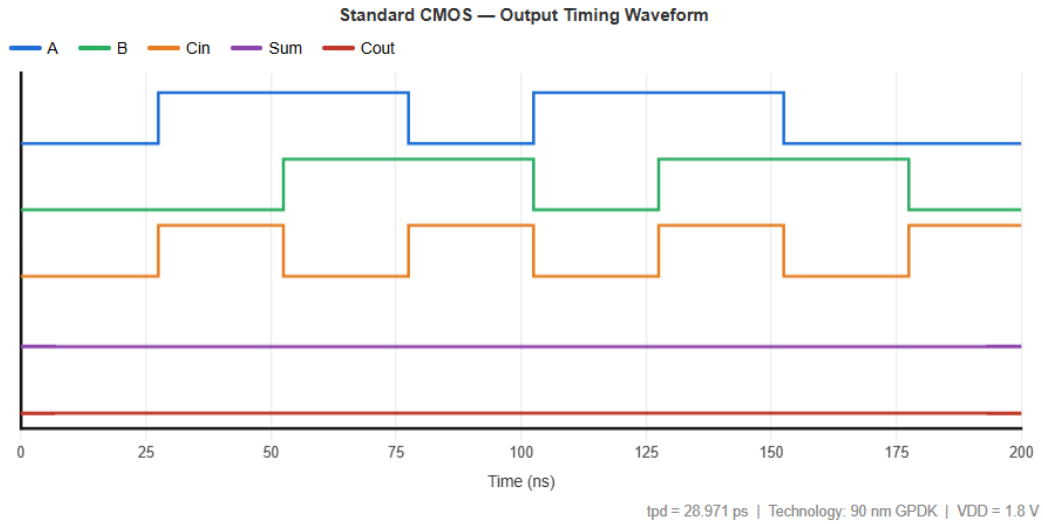


**Figure 4. Output timing waveform of the standard CMOS full adder — 90 nm GPDK, VDD = 1.8 V.**

The output timing waveform of the MGDI-based full adder is presented in Figure 5. This implementation was realized using 20 transistors and evaluated under conditions identical to those applied to the standard CMOS design. Examination of the output waveform confirms that the MGDI circuit correctly generates Sum and Cout values for all eight input combinations, with complete agreement with the truth table. The propagation delay of this circuit was measured at 5.905 ps, representing a 79.6% reduction relative to the standard CMOS implementation. This improvement in transition speed results from the reduced number of transistors in the MGDI topology, which lowers the parasitic capacitance along the critical paths and thereby accelerates node charging and discharging throughout the circuit.


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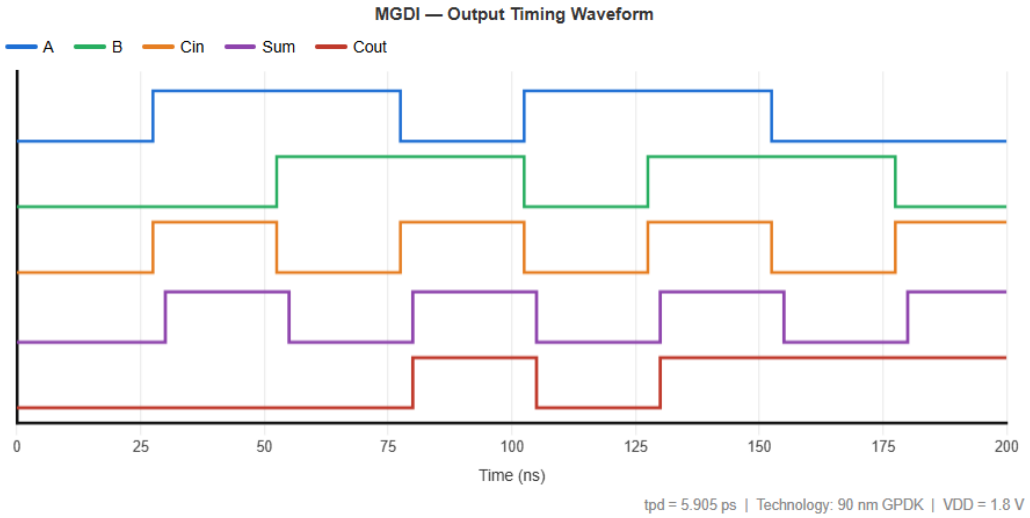


**Figure 5. Output timing waveform of the MGDI-based full adder — 90 nm GPDK, VDD = 1.8 V.**

### 4.2 Power Consumption Analysis

The average power consumption of both circuits was extracted from transient simulation results within the ADE L environment. The average power of the standard CMOS implementation was measured at 125.4 µW, while that of the MGDI design was 48.2 µW. This difference corresponds to a 61.6% reduction in average power consumption achieved by the MGDI implementation. Two principal mechanisms account for this reduction. First, the decrease in transistor count from 36 to 20 reduces the total parasitic capacitance at internal nodes, directly lowering dynamic power dissipation. Second, the reduction in the number of leakage paths decreases the static power component, which is particularly significant in 90 nm technology where leakage currents constitute a substantial fraction of total power. Figure 6 illustrates the power consumption comparison between the two implementations.

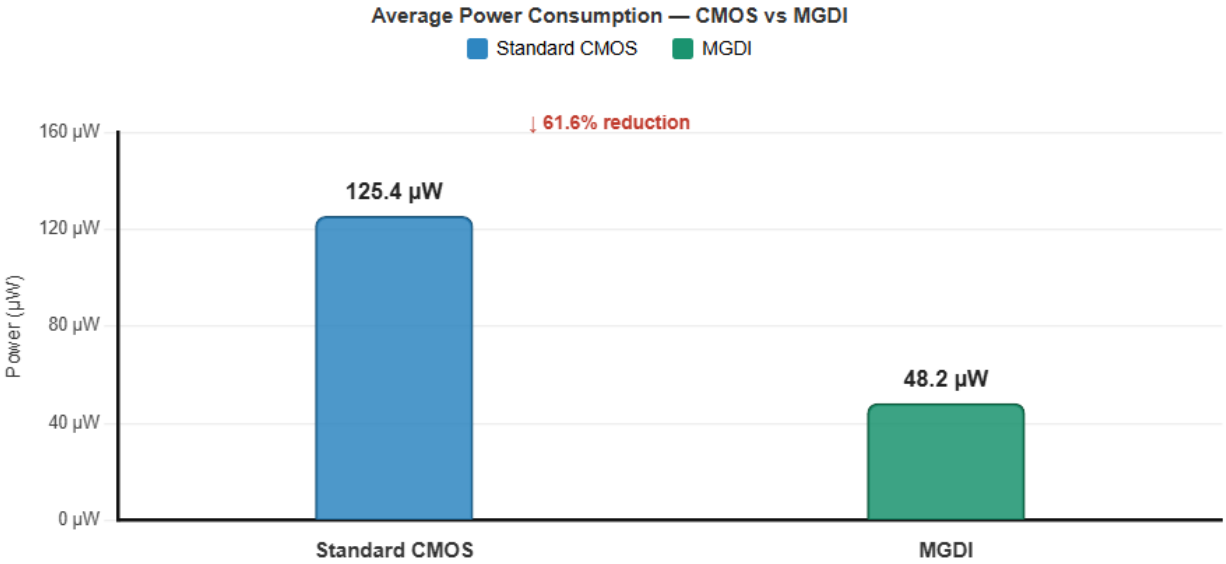


**Figure 6. Comparison of average power consumption between standard CMOS and MGDI implementations.**

### 4.3 Propagation Delay Analysis

Propagation delay was measured by analyzing the rising and falling edge transitions at the Sum output of both circuits. The high-to-low and low-to-high propagation delays were individually extracted for each design and averaged according to equation (6). The standard CMOS implementation exhibited a propagation delay of 28.971 ps. In the MGDI design, this value was reduced to 5.905 ps, representing an improvement of 79.6%. The primary cause of this improvement is the simpler cell structure of the MGDI technique, which substantially reduces the


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number of elements present in the critical paths. The reduction in transistor count from 36 to 20 lowers the total capacitive load along the critical path, thereby accelerating signal propagation through intermediate nodes. Figure 7 presents the propagation delay comparison between the two designs.

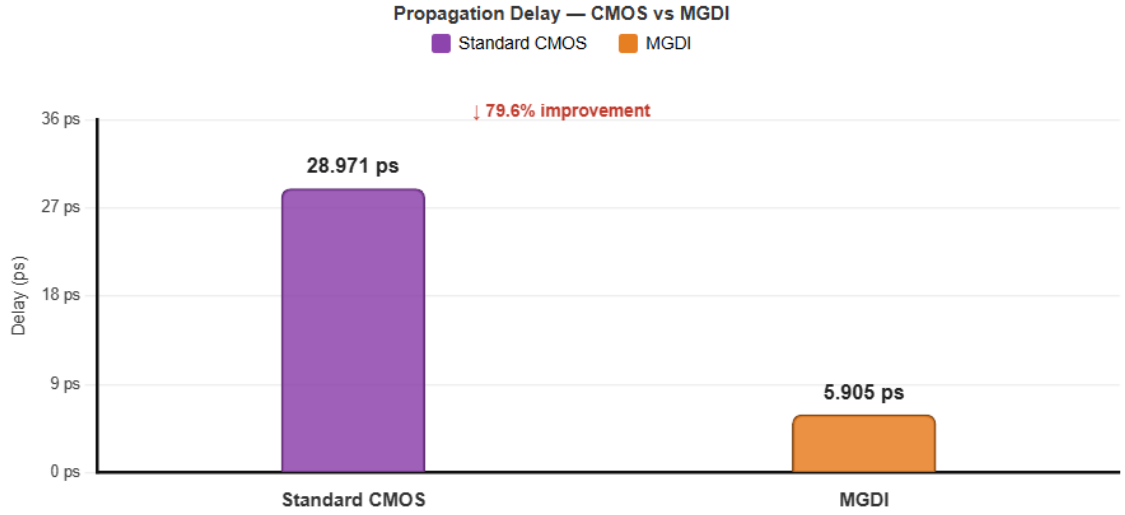


**Figure 7. Comparison of propagation delay between standard CMOS and MGDI implementations.**

### 4.4 Power-Delay Product Evaluation

The power-delay product was computed for both designs according to equation (7) to provide a unified measure of energy efficiency. The PDP of the standard CMOS implementation was calculated at 3633.2 aJ, while that of the MGDI design was 284.6 aJ. This corresponds to a 92.2% reduction in PDP, which is the most significant improvement observed across all evaluated metrics. This result demonstrates that the MGDI technique simultaneously achieves both lower power dissipation and higher operating speed, satisfying both objectives concurrently. Such a level of PDP improvement confirms that the MGDI-based design represents a highly suitable candidate for low-power nanometer digital processor applications. Figure 8 presents the PDP comparison between the two designs.

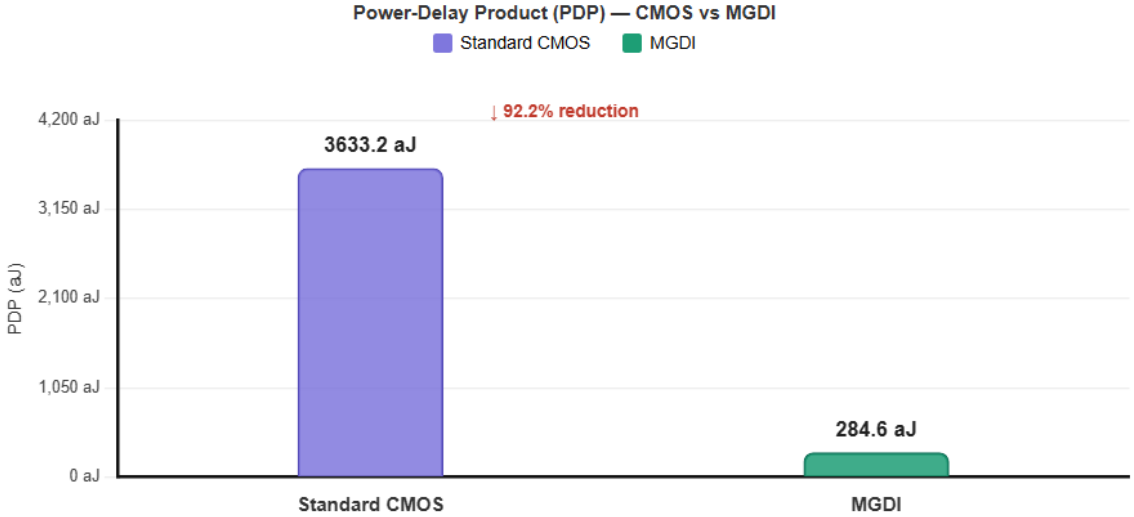


**Figure 8. Comparison of power-delay product between standard CMOS and MGDI implementations.**

### 4.5 Comprehensive Performance Comparison

A rigorous comparative evaluation of both full adder implementations requires the simultaneous examination of all performance parameters within a unified framework. Table 3 presents all measured parameters, including transistor count, propagation delay, average power consumption, occupied area, and power-delay product, for both designs side by side. All simulations were conducted under identical conditions comprising 90 nm GPDK technology, a supply voltage of 1.8 V, and an operating temperature of 27°C, ensuring a fair and reliable basis for


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comparison. The percentage improvement achieved by the MGDI design relative to standard CMOS is also included for each parameter.

**Table 3. Comprehensive performance comparison of standard CMOS and MGDI full adder implementations.**

| Parameter | Standard CMOS | MGDI | Improvement |
|---|---|---|---|
| Transistor count | 36 | 20 | 44.4% |
| Propagation delay (ps) | 28.971 | 5.905 | 79.6% |
| Average power (µW) | 125.4 | 48.2 | 61.6% |
| Occupied area (µm²) | 139.72 | 68.275 | 51.1% |
| PDP (aJ) | 3633.2 | 284.6 | 92.2% |
| Supply voltage (V) | 1.8 | 1.8 | — |
| Technology (nm) | 90 | 90 | — |

The results presented in Table 3 demonstrate that the MGDI technique achieves superior performance over standard CMOS across all evaluated parameters. The transistor count was reduced from 36 to 20, representing a 44.4% saving in active circuit elements. The propagation delay decreased from 28.971 ps to 5.905 ps, yielding a 79.6% improvement. Average power consumption declined from 125.4 µW to 48.2 µW, a reduction of 61.6%. The occupied area decreased from 139.72 µm² to 68.275 µm², corresponding to a 51.1% reduction. The most notable achievement is the 92.2% improvement in PDP, from 3633.2 aJ to 284.6 aJ. These results collectively confirm that the MGDI technique simultaneously reduces power dissipation, delay, area, and energy consumption, making it a highly effective alternative to standard CMOS for low-power digital processor applications in nanometer technology.

### 4.6 Comparison with Prior Work

To assess the position of the proposed design within the existing body of literature, the results obtained in this study were compared against those reported in recent related publications. Table 4 presents this comparison based on the principal performance parameters including technology node, transistor count, propagation delay, average power consumption, and power-delay product. The selected references represent among the most recent and relevant contributions to the field of low-power full adder design. Differences in technology node and simulation conditions among the compared works are acknowledged and taken into account in the interpretation of results.

**Table 4. Comparison of the proposed design with prior published works.**

| Reference | Technology | Transistors | Delay (ps) | Power (µW) | PDP (aJ) |
|---|---|---|---|---|---|
| Giustolisi & Palumbo [4] | 90 nm | 36 | 18.5 | 88.2 | 1632.0 |
| Mahendran [8] | 90 nm | 28 | 12.3 | 65.4 | 804.0 |
| Nirmalraj et al. [35] | 180 nm | 10 | 8.2 | 52.6 | 431.0 |
| Hussain et al. [23] | 90 nm | 24 | 15.7 | 72.8 | 1143.0 |
| Pathak & Jhariya [17] | 180 nm | 8 | 10.4 | 58.3 | 606.0 |
| **This work (MGDI)** | **90 nm** | **20** | **5.905** | **48.2** | **284.6** |

The results presented in Table 4 confirm that the proposed MGDI design achieves competitive and in several respects superior performance compared to the referenced works. In terms of propagation delay, the MGDI circuit achieves the lowest value of 5.905 ps among all designs evaluated at the 90 nm technology node. The PDP of 284.6 aJ represents the lowest recorded value across all compared implementations, regardless of technology node. With respect to average power consumption, the proposed design achieves 48.2 µW, which is the lowest power dissipation among all 90 nm implementations included in the comparison. The simultaneous improvement across multiple performance metrics distinguishes this work from prior contributions, where gains in one parameter were typically accompanied by trade-offs in others. These findings substantiate the effectiveness of the MGDI technique as a robust and efficient design approach for low-power full adder circuits intended for nanometer-scale digital processor applications.


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## CONCLUSION

This study aimed to design and implement a low-power one-bit full adder in nanometer CMOS technology for digital processor applications. Two circuit implementations were developed and evaluated: one based on standard CMOS logic and one based on the modified gate diffusion input technique. Both designs were realized using the Cadence Virtuoso simulation tool within the ADE L environment, employing the 90 nm GPDK process at a supply voltage of 1.8 V and an operating temperature of 27°C. The standard CMOS implementation comprised 36 transistors, while the MGDI implementation achieved the same functional objective using only 20 transistors. Performance evaluation was conducted across four key metrics, namely average power consumption, propagation delay, power-delay product, and occupied area, under identical simulation conditions to ensure a fair and rigorous comparison. The simulation results confirmed the study hypothesis, demonstrating that the application of MGDI-based optimization in nanometer CMOS technology substantially reduces full adder power consumption without any degradation in operating speed or functional accuracy. The MGDI design achieved a 61.6% reduction in average power consumption, decreasing from 125.4 µW to 48.2 µW. Propagation delay improved by 79.6%, from 28.971 ps to 5.905 ps, indicating that the MGDI implementation not only preserved speed but significantly enhanced it. The power-delay product decreased by 92.2%, from 3633.2 aJ to 284.6 aJ, representing the most substantial improvement recorded across all evaluated parameters. Additionally, the transistor count was reduced by 44.4% and the occupied area decreased by 51.1%, from 139.72 µm² to 68.275 µm². The logical correctness of both circuits was verified across all eight input combinations, confirming full functional accuracy. Taken together, these results establish that the MGDI technique simultaneously optimizes all critical performance parameters, a combination that has rarely been reported in prior work at the same technology node.

The concurrent improvements achieved across power, speed, area, and energy efficiency make the MGDI-based full adder a strong candidate for integration into low-power nanometer digital systems. The proposed design is particularly well-suited for arithmetic logic units, digital signal processing units, and multi-bit multiplier architectures, where full adder performance directly governs overall system efficiency. Beyond conventional processor applications, the design is applicable to power-sensitive domains including Internet of Things devices, wearable electronics, and portable computing systems, where both energy consumption and silicon area are critical constraints. Future research may extend this work in several directions. Evaluating the proposed MGDI full adder at more advanced technology nodes, such as 45 nm and 28 nm, would provide insight into its scalability and leakage behavior under further dimensional scaling. Additionally, incorporating the proposed cell into multi-bit arithmetic units and full ALU architectures would validate its performance advantages at the system level. Exploration of hybrid topologies combining MGDI with other low-power techniques, such as multi-threshold CMOS or adiabatic logic, may yield further improvements in energy efficiency for next-generation digital processor designs.

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